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Digitally Controlled Bridgeless Totem-Pole Power Factor Corrector

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A B S T R A C T

This paper presents the steps of designing, controlling, and implementing a 3kW Gallium-Nitride (GaN)-based bridgeless totem-pole power factor corrector (PFC) for single-phase 230V rectifier applications. The bridgeless design of such a converter combined with zero-recovery switching loss of GaN transistors enables more efficient design operation compared to traditional Si-based solutions. Thermally efficient design with forced-air cooling for the switching devices increased the power density beyond 100W/inch3 while keeping the power switches temperatures less than the thermal limits. Continuous Conduction Mode (CCM) was adopted in this work for better converter stability and was analyzed thoroughly along with the losses breakdown for each part of the converter. The digital control model of the converter was discussed in detail accompanied by the hardware design steps for the converter. Experimental results proved a maximum efficiency of 98.9% during 2.4kW operation and 98.6% during 3kW (full load) operation with minimum Total Harmonics Distortion (THD) of AC input current of 2.78% at rated current (13A) when converting the AC input voltage (230V) to 400 VDC.

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مصحح عامل القدرة للمحول الغير مجسر ذي القطب الخاضع للتحكم رقميًا

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الخلاصة

يقدم هذا البحث خطوات تصميم، والتحكم، وتنفيذ مصحح عامل القدرة (PFC) القائم على الجاليوم-نيتريد (GaN) بقدرة 3 كيلو وات لتطبيقات مقوم 230 فولت أحادي الطور. يتيح التصميم غير الجسور لمثل هذا المحول جنبًا إلى جنب مع فقدان تبديل الاسترداد الصفري لترانزستورات GaN تشغيل تصميم أكثر كفاءة مقارنة بالحلول التقليدية القائمة على Si. يعمل التصميم الفعال حرارياً مع التبريد بالهواء القسري لأجهزة التبديل على زيادة كثافة الطاقة التي تتجاوز 100 واط / بوصة 3 مع الحفاظ على درجات حرارة مفاتيح الطاقة أقل من الحدود الحرارية. تم اعتماد وضع التوصيل المستمر (CCM) في هذا العمل لتحسين استقرار المحول ويتم تحليله بدقة إلى جانب توزيع الخسائر لكل جزء من المحول. تتم مناقشة نموذج التحكم الرقمي للمحول بالتفصيل مصحوبًا بخطوات تصميم الأجهزة للمحول. أثبتت النتائج التجريبية كفاءة قصوى بلغت 98.9٪ أثناء تشغيل 2.4 كيلو وات و98.6٪ أثناء تشغيل 3 كيلو وات (حمولة كاملة) مع الحد الأدنى من التشوه التوافقي الكلي (THD) لتيار إدخال التيار المتردد بنسبة 2.78٪ عند التيار المقنن (13 أمبير) عند تحويل جهد دخل التيار المتردد (230 فولت) إلى 400 فولت تيار مستمر.

الكلمات الدالة: عامل تصحيح القدرة، كاليون نتراید، المحول الغير مجسر ذي القطب، الاتصال المستمر، تضمين عرض النبضة.

1.INTRODUCTION

Conventional Power Factor Correction (PFC) converters incorporate a full-bridge diode rectifier at the AC input stage followed by a boost converter stage s to raise the AC rectified voltage level to achieve power factor correction functionality [1, 2]. The boost part of such converters is usually a Si-based high-frequency MOSFET or IGBT depending on the power level and the application it is used in as shown in Fig. 1 [3]. Using a full-bridge diode rectifier resulted in high conduction losses in the pre-boost rectifier stage. Therefore, in more recent realizations of PFC converters, a configuration in which the diode rectifiers are replaced by the boosting power switches [4]. Thus, combining the two rectifiers and the boost stage into a single stage is known as. bridgeless. as shown in Fig. 2 [5, 6].

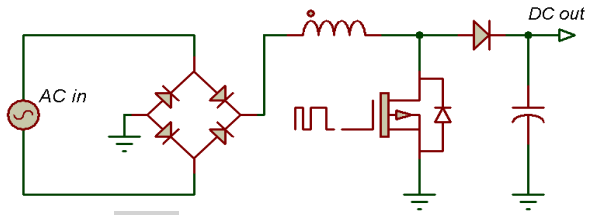


Fig.1 Traditional PFC circuit.

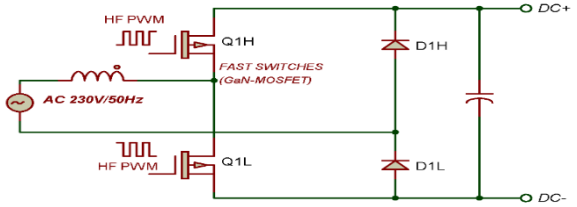


Fig.2 Bridgeless PFC circuits.

Despite the vast improvements of using bridgeless topology as in Fig.1, this design still has serious issues represented by the losses due to the reverse recovery associated with Si-based MOSFETs [7, 8]. The bridgeless totem-pole PFC presented in this paper has been well-studied in papers but has not been widely embraced due to the above-mentioned reverse recovery losses issue by using conventional Si-based power switches. The fact that GaN devices have zero reverse recovery loss, makes them an efficient and attractive solution to this particular PFC topology. Moreover, by using this topology, Si-based power devices (MOSFETs) are used in slow line frequency (50H/60Hz) rectification (Q2H and Q2L in Fig. 1). The use of traditional Si-based switches has many benefits including the great reduction in switching losses by using low- frequency (line frequency) and fewer conduction losses compared to the diodes used in semi-bridgeless or traditional PFC circuit that uses full-bridge diode rectifier. The other benefit of using such a configuration is that the high-frequency GaN devices allow the alternation of the upper (Q1H) and the lower (Q1L) in operation as a boost switch or as a synchronous diode in the positive and negative half of the AC waveform respectively. As a result, enhance the utilization of switches compared to the conventional PFC topology. Another benefit of using this PFC configuration is its ability to reverse the direction of the power flow from a grid to a DC bus (PFC boost rectifier) or from a DC bus to a grid (grid-connected inverter). Therefore, this totem-pole PFC topology becomes an appealing choice for Electric Vehicles (EV) chargers that

allow bidirectional power flow from Vehicle to Grid (V2G) or from Grid to Vehicle (G2V) besides high-efficiency DC/AC motor drives rectifier stage. In this paper, the analysis and hardware design steps with the control strategy are presented [9, 10].

2.TOTEM POLE PFC OPERATION

As illustrated in Fig. 3 (top), the Q1L acts as a high-frequency (100 kHz) switch that charges the inductor at a switching frequency rate with duty cycle, D that depends on the current position decided by a current controller (TON). After the duty time of Q1L is finished, as shown in Fig. 3 (bottom) then the upper high-speed GaN transistor, Q1H is turned on for the rest of the duty time (TOFF) to discharge the energy from the PFC inductor. As a result, the DC voltage at the output equals the input voltage plus the voltage generated by the inductor due to the current change with time (di/dt). This means the DC output voltage depends on the charging time ratio of the inductor or duty cycle, D. Q2L remains on for the whole half AC cycle.

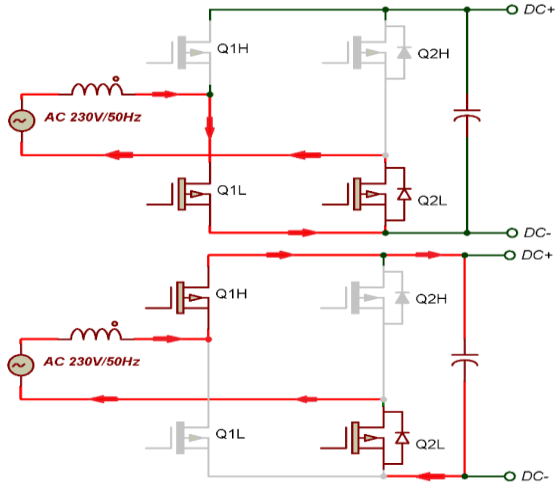


Fig.3 Operation of totem-pole PFC in CCM mode during the positive-half AC cycle showing inductor charging (top) and discharging(bottom).

Similarly, during the negative-half cycle, the low-frequency Si-based power switch, Q2H remains on. As shown in Fig. 4. (top), the high-speed GaN power switch Q1H is now responsible for the inductor charging instead of Q1L in the positive-half AC cycle. A similar concept for the charging time of the inductor is applied for the positive half, i.e., the TON time to the total switching time ratio, D is decided by the current controller to force the average inductor current to follow the generated sinusoidal current reference. The inductor is discharged by turning the lower high-speed GaN MOSFET, Q1L. this allows the discharging of the stored energy in the inductor through it and thus, provides boosting for the input AC voltage during the negative-half cycle.

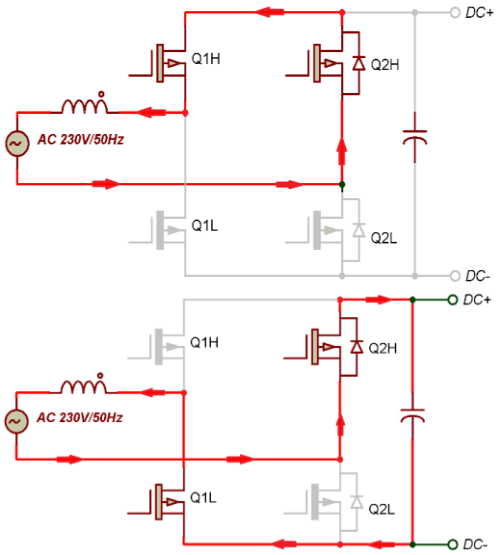


Fig.4 Totem-pole PFC in CCM mode during the negative-half AC cycle.

3.TOTEM POLE PFC HARDWARE DESIGN

Fig. 5 Shows the basic block diagram of the designed system prototype.

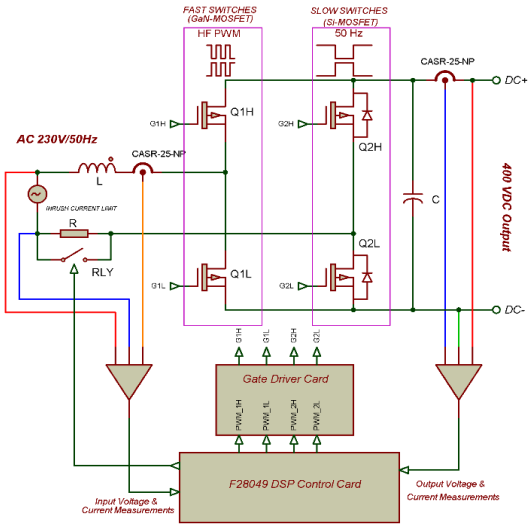


Fig.5 Simplified block diagram of 3 kW prototype totem-pole PFC.

The key specifications of the designed converter are listed in Table 1.

Table 1. Designed System Key Specifications

Parameter	Specification
AC Input Voltage	110 to 230 V (RMS), 50 to 60 Hz
AC Input Current	18 A (RMS)
DC Output Voltage	400 V (DC)
DC Output Current	7.5 A (DC)
Rated Output Power	3 kW (230 V AC input), 2kW (110 V AC Input)
DC Output Ripple	8 Vpp
Switching Frequency	100 kHz
Peak Efficiency	98.9 %
Peak Current THD	2.78 %
PFC Inductor	220 µH
Output Capacitors	1780 µF
High-Frequency GaN MOSFETS	TP65H035G4WS (TRANSPHORM)
Low-Frequency Si MOSFETs	STY139N65M5

3.1.Inductor Design

The totem-pole PFC inductor is designed to keep the current ripple within 25% of the peak AC input current, Iin_pk. Keeping in mind that the maximum input current is calculated at the minimum input voltage of the converter at full designed load, Equation (1) gives the minimum inductance value required to operate the PFC in CCM mode [11].

$$L_{min} = \frac{(D-D^2)V_{out}V_{in\_min}}{0.25\sqrt{2}P_{out}F_{sw}} \quad \text{..... (1)}$$

Where D is the average duty cycle of the high-speed GaN MOSFETs (Q1H&Q1L) and is calculated approximately as in [8] to be 0.425. V_{out} is the PFC DC output voltage (400VDC). Pout is the nominal output power of the PFC converter (3 kW). V_{in_min} is the minimum AC input voltage, which is 110 VAC to operate the designed converter in both 230/115 VAC single-phase grid standards. Fsw represents the switching frequency of the converter which has been chosen to be 100 kHz to fairly utilize the high-speed capability of the GaN power switches. Using the above definitions in Equation (1), the minimum inductance value is 106 µH. Using the Kool Mµ core (from Magnetics), 40 turns will produce an inductance of 220 µH at full load to further ensure CCM operation even in surge conditions. The windings of the inductor are formed by 2 strands of the AWG-12 wire size.

3.2.Output DC-Link Capacitor Design

The output DC-link capacitor value can be obtained by knowing the DC voltage maximum holding-up time at full-load, t_{hu}, and the desired output DC voltage ripple, V_{ripple}. t_{hu} is set to a half AC cycle, or 10 ms, while the voltage ripple is selected to be 2% or 8Vpp. The output capacitor can be calculated by Equation (2)

$$C_{out} = \frac{2\times P_{out}\times t_{hu}}{V_{out}^2 - V_{out\_min}^2} \quad \text{..... (2)}$$

$$C_{out} = \frac{P_{out}}{2\times V_{out}\times 2f_{line}\times V_{ripple}} \quad \text{..... (3)}$$

Using Equations (2) and (3), the output DC-link capacitor value equals 1492 µF. three Vishay 57561E3, 560 µF, 450V output DC-link electrolytic capacitors were used in parallel with 100 µF, 500V ceramic Multi-Layer Capacitor (MLC) (Vishay MKP1848M) for better high-frequency ripples suppression.

3.3.Inrush Current Limit and Soft Start

Since the output capacitors are fairly large, charging these capacitors requires a current-limiting circuit to avoid the high-current stress on the AC line and input fuse and filter. This pre-charging is done by the built-in free-wheeling diodes in power switches before the PFC function is enabled at startup by inserting a resistor in series with the AC input. This resistor is then shorted by a power relay after the capacitors are being charged to a specific voltage level as shown in Fig. 5 A 10Ω TE Connectivity, SQMW710RJ is used.

3.4.High-Speed GaN MOSFET Selection

Fig.6 shows the structure of the selected normally-off GaN power switch packed in a standard TO247 package. The main (upper) GaN FET has a low RDS(ON), avalanche ruggedness, and low switching losses [12]. The lower low-voltage Si-based MOSFET is connected between the GaN FET and the module sources that control the VGS of the GaN module. This low-voltage MOSFET is responsible for controlling both di/dt and dv/dt during turning off and on respectively thanks to its external gate resistor. Since the Si-based MOSFET is a low voltage, it has an extremely low RDS(ON) resistance and a negligible reverse recovery charge (Qrr) [13]. Therefore, the GaN module can be driven by a single 12V supply gate-driver circuit. Thus, simplifying the driver requirements and reducing the total system cost compared to the SiC MOSFETs that require a bipolar gate-to-source voltage [14]. Combining all the above-mentioned features, the TRANSPHORM TP65H035G4WS GaN power switch is selected.

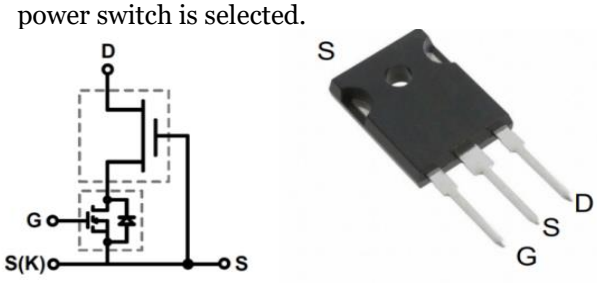


Fig.6. Normally-off TPH3205WS GaN power switch internal structure.

3.5.Low-Speed Si-MOSFET Selection

Because of the low-speed switching patterns (line frequency) in the totem pole PFC for Q2H and Q2L in Fig. 5, the switching losses are negligible. Only conduction loss is taken into consideration so, regardless of the transient performance of any power switch, the lower the RDS(ON) resistance the better the design is concerning thermal performance and efficiency. The STY139N65M5 has a reasonable on-state resistance (0.014 Ω) per cost and thus, is selected as a slow-switching power device for the system.

4.LOSS CALCULATION AND THERMAL BREAKDOWN

The total system losses are calculated by full system-rated load and can be divided into four categories, which are:

4.1.Losses of GaN Power Switches

Conduction Loss for the two GaN switches can be found using Equation (4):

$$P_{cond\_GaN} = I_{rms}^2 \times R_{DS(ON)\_GaN} \quad \text{... (4)}$$

Referring to the part datasheet for $R_{DS(ON)}$ (35 mΩ) and Table I., for RMS input current (18 A), the conduction loss is 11.34 W. The switching losses for GaN MOSFETs are calculated using Equation (5):

$$P_{sw\_GaN} = F_{SW} \times E_{oss\_GaN} \quad \text{..... (5)}$$

Where E_{ossGaN} is the total energy loss at full load (18 Arms) current, which is 140 µJ, the switching losses are found to be 14 W for the two GaN devices because they conduct in a complementary manner, so, full input AC current is flowing in either Q1L or Q1H. as a result, they can be dealt with as one always-on transistor. The same principle is applied to slow switches, Q2L and Q1H.

4.2.Losses of Si-MOSFET Power Switches

The conduction Loss for the upper and lower Si-MOSFET switches can be found using Equation 4. The total loss is calculated to be 4.5 W.

4.3.Losses of Boost Inductor and Output Capacitors

Output capacitor losses can be found using Equation (6):

$$P_{loss\_cap} = \frac{R_{esr\_cap} \times \Delta i^2}{3} \quad \text{..... (6)}$$

Where R_{esr_cap} is the Equivalent Series Resistor (ESR) of the used capacitors (380 mΩ from part no. datasheet) and Δi is the output current ripple at full load which is the voltage ripple previously calculated in output capacitor design (8Vpp) divided by the equivalent load resistance (400V2/3kW = 53.33 Ω). Keeping in mind that there are three parallel capacitors used in the system, the power loss for output capacitors is 2.85W. The power loss of the boost PFC inductor is calculated using Equation (7):

$$P_{loss\_inductor} = I_{rms}^2 \times R_{esr\_inductor} \text{ ... (7)}$$

Using inductor core geometry from the datasheet, the total wire length of the PFC inductor is 2.4 m, and the DC resistance is found to be 12.5 mΩ. Neglecting the AC resistance due to skin effect magnetic core losses, the power loss in the inductor is 4W.

4.4.Control and Auxilliary Circuit Power Consumption

The power drawn by the microcontroller card, gate driver card, and other measurement circuits is measured to be 6W by measuring the current of the main 12V adapter powering the whole system. Combining all the losses calculated above, the total system losses during full load operation are 42.7 W. Therefore, the theoretical efficiency is 98.597%. Fig. 7 shows the loss contributed by the different parts of the system.

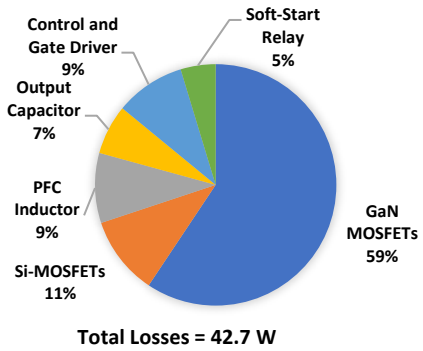


Fig.7 Breakdown of major contributors to system losses.

5.TOTEM-POLE PFC CONTROL STRUCTURE

The average AC input current control method mentioned is widely used as a control strategy for single-phase classical topology [15, 16]. The control structure for the prosed system is shown in Fig. 8. The control method is modified to convert the single PWM gate driver signal originally aimed to control the topology shown in Fig. 1.

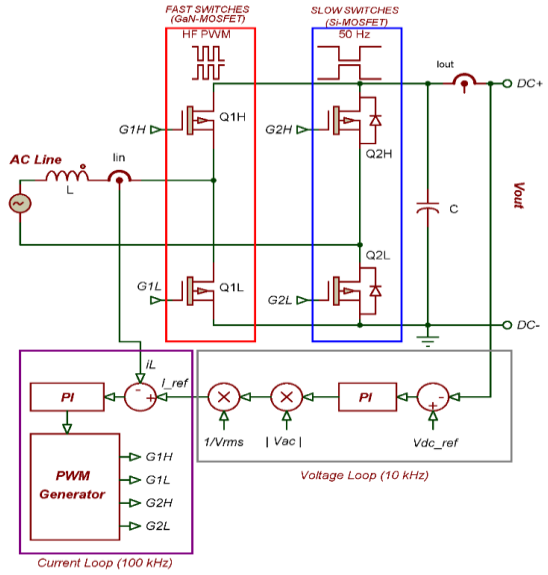


Fig.8 Modified control structure for the proposed system.

In this control method, the output DC voltage is controlled by the outer voltage loop that runs relatively slow (10 kHz) compared to the inner loop. A feed-forward signal represented the absolute value of the instantaneous input AC voltage. The signal is then divided by the square RMS value of the AC to form the desired input AC current reference [17, 18]. The current reference generated by the outer voltage loop and feed-forward parameters is then fed to the inner loop to be compared against the actual inductor current (AC line current) to form the current error signal. This error signal is then input to a Proportional-Integral (PI) controller to adjust the duty cycle to force the AC input

current to be sinusoidal [19]. As mentioned before, the duty ratio is converted from one high-frequency (100 kHz) to four PWM signals; two of which are high-frequency complementary signals that switch places according to the AC waveform half and the other two PWM signals are low-frequency (AC line frequency) generated by the zero-crossing detector as shown in Fig. 9.

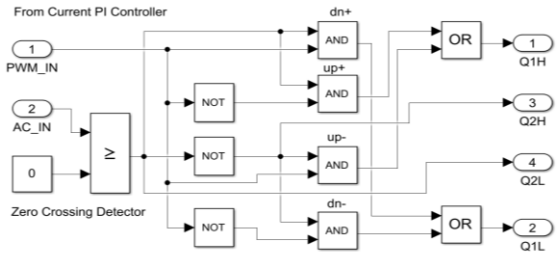


Fig.9 Controller PWM modification to convert classical single to four-PWM totem-pole PFC controller.

6.PRACTICAL IMPLEMENTATION

6.1.Power Board

The implemented power board is shown in Fig. 10. and is composed of GaN and Si MOSFETs with an AC input filter, boost PFC inductor, output capacitors, and current/voltage measurement circuits as shown in the circuit in Fig. 13. The power board is designed using four-layer PCB scheme, the complete assembled board is shown in Fig. 11.

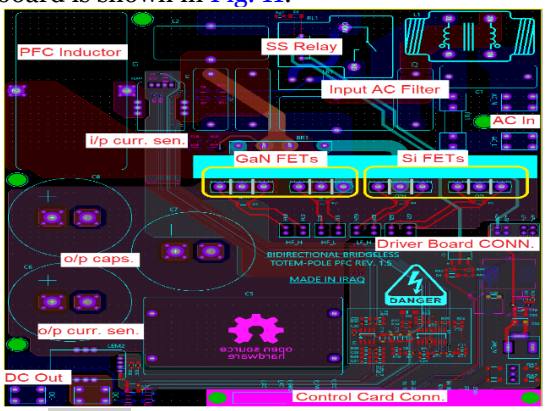


Fig.10 Power card of totem-pole PFC.

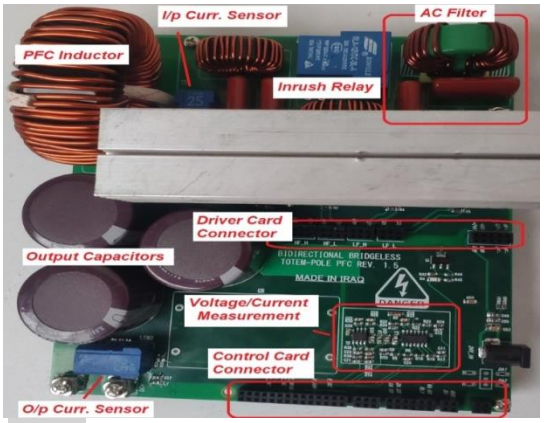
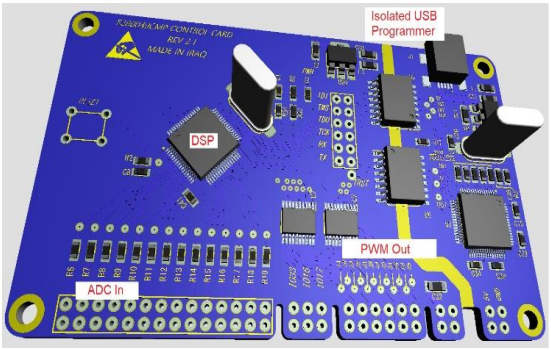


Fig.11 Power card of the designed bridgeless totem-pole PFC.

6.2.Controller Board

The controller card is shown in Fig. 12, The design is based on the new TI DSP and F280049CPM. The controller board also contains a built-in XDS100 V2 programmer/debugger with a completely isolated USB interface for safely accessing the board during normal operation. The control card 3d and real views are shown in Fig. 12.



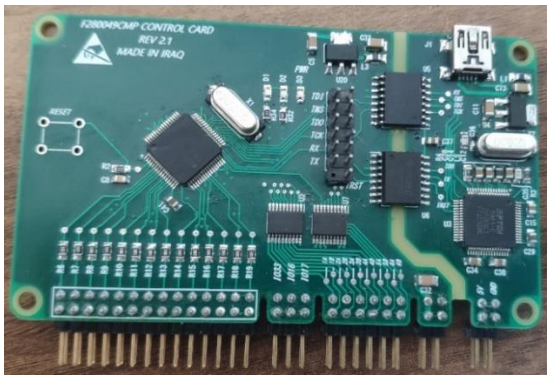


Fig.12 Control card of the designed system.

6.3.Gate Driver Board

The gate driver board handles the PWM signals boosting from MCU and translates the 3.3V level voltages to a compatible level (0-to-12V) to turn the SI and GaN MOSFETs on or off. It is based on the isolated driver topology which means there is full galvanic isolation between the power part of the system and the low-voltage control part. The implemented gate driver board is shown in Fig. 14. The 3d view of the gate driver board is shown in Fig. 15. The complete schematic of the driver card is shown in Fig. 16.

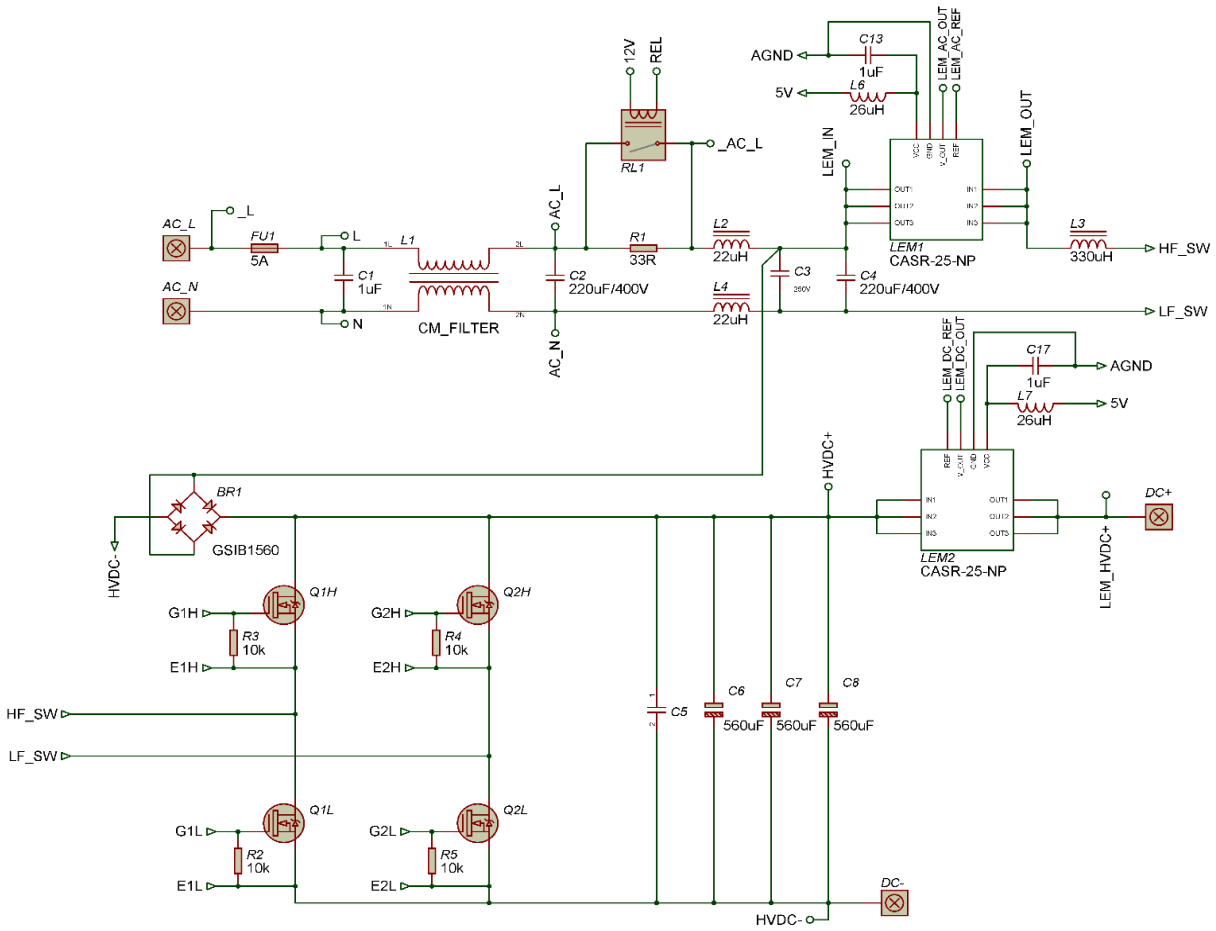


Fig.13 Power card basic circuit diagram.

Fig.14 Driver card for the designed system.

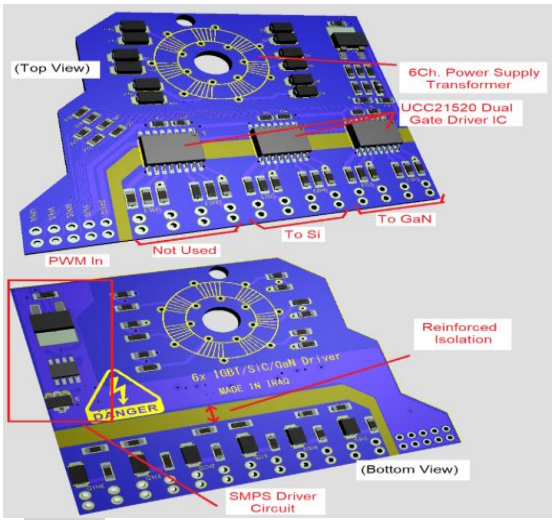


Fig.15 Driver card for the designed system.

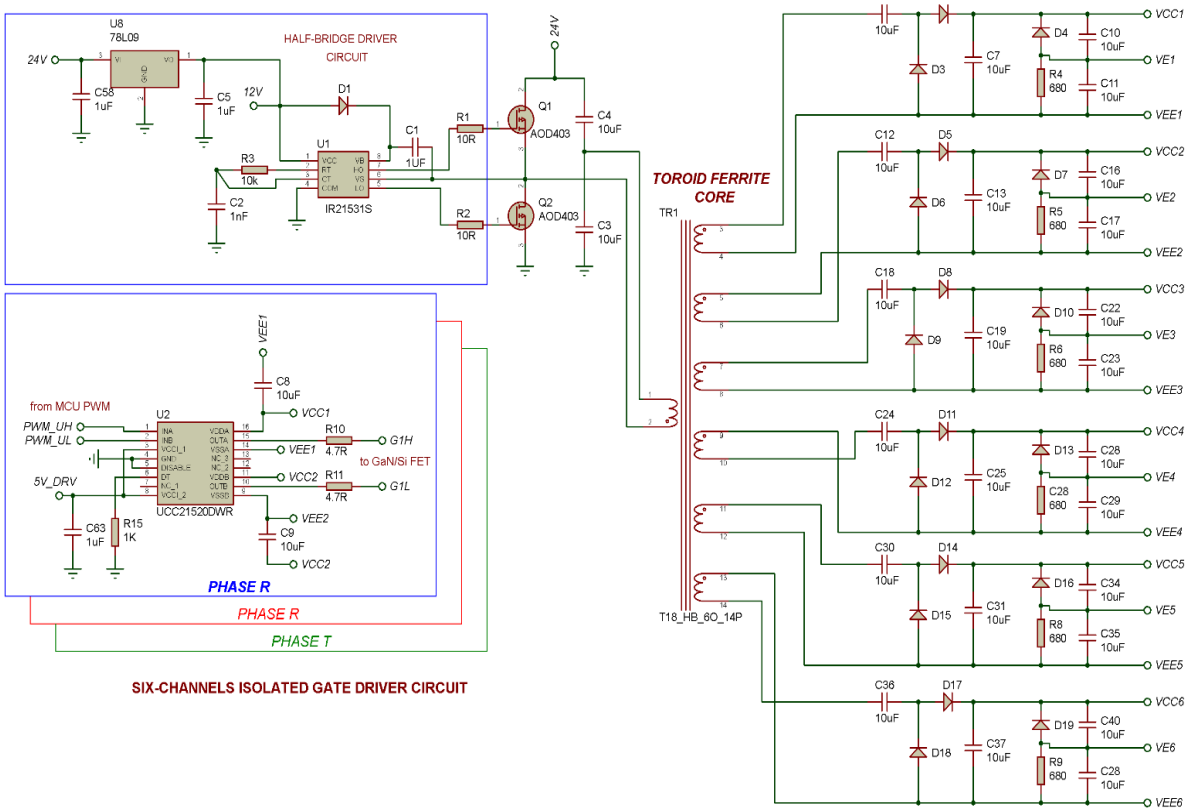


Fig.16 Driver card schematic.

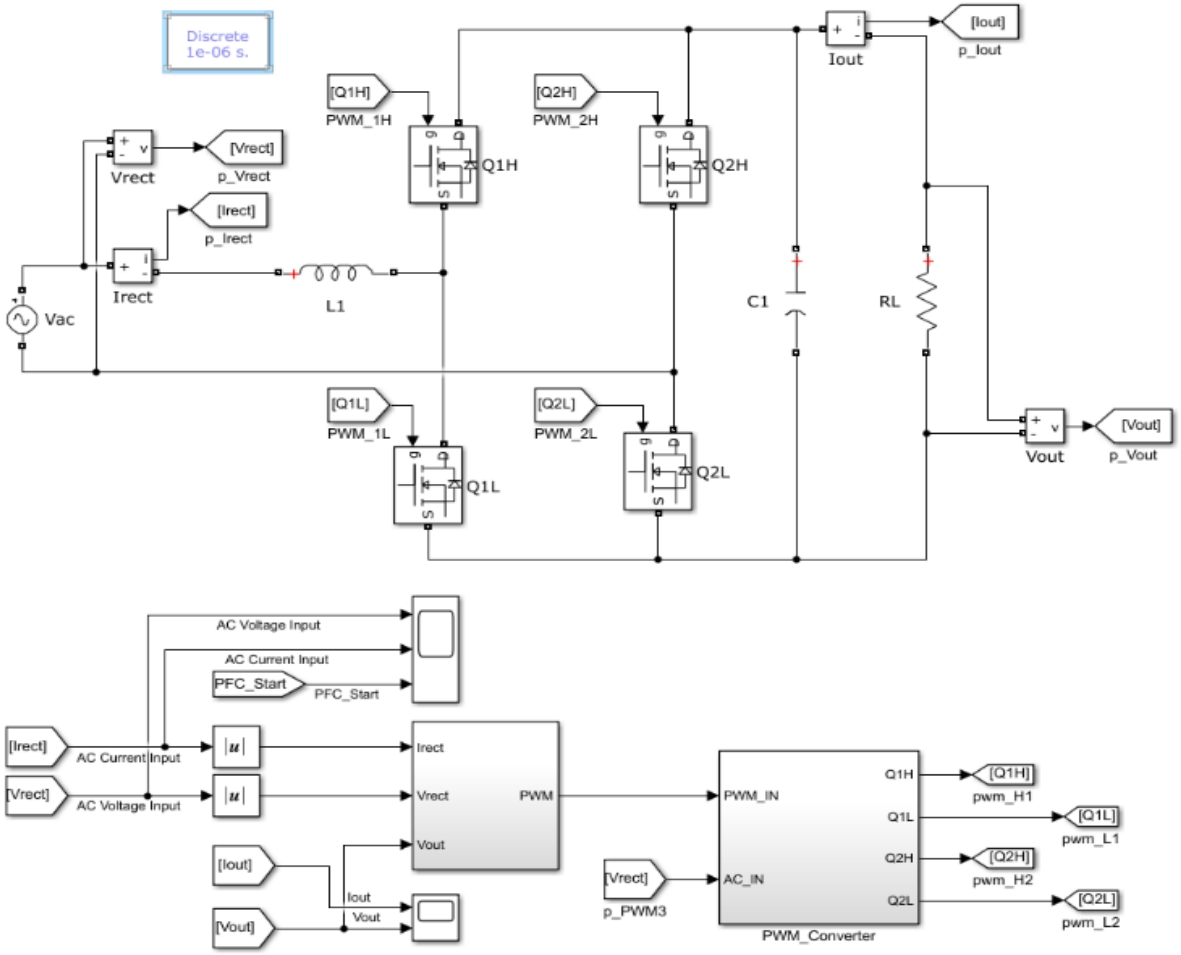


Fig.17 MATLAB simulation of the bridgeless totem-pole PFC.

7.SIMULATION RESULTS

The simulation of the designed system is performed using MATLAB/SIMULINK. Fig. 17 Shows the main simulation block diagram. The controller block inner structure is shown in Fig. 18 and is tuned using the built-in PID tuning app in MATLAB/SIMULINK. The P for the term for the outer voltage loop is 3.0, while the I term is 1.8. for the inner current loop, the P term is 1500 and the I term is 50 [20, 21]. The PFC controller is started after 0.05 sec to demonstrate the AC current waveform before and after the PFC function started. Fig. 19 Shows the AC current waveform at full load before and after the PFC controller activation. The AC current THD is 108% before the PFC function is activated, after activation (at t = 0.05 sec), the THD became 2.8% (measured using SIMULINK THD measurement block). DC output voltage ripples were 10 V_{pp}[22].

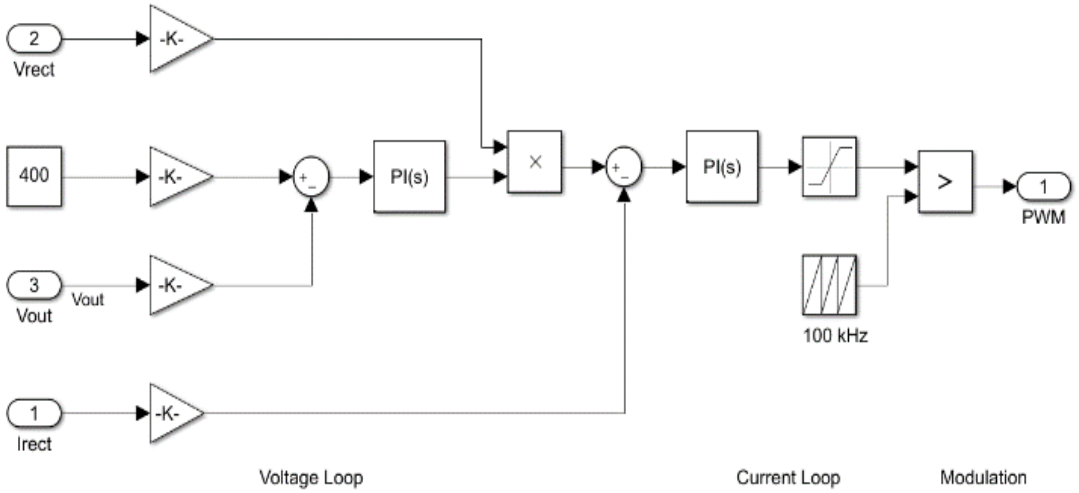


Fig.18 PFC controller simulation in MATLAB/SIMULINK

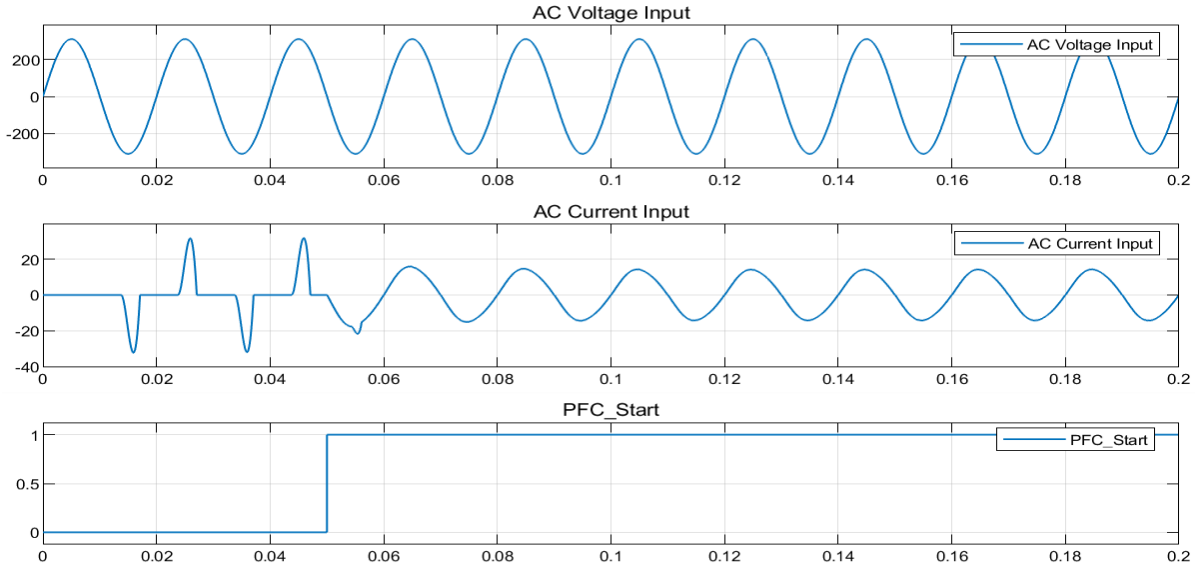


Fig. 19 PFC input AC voltage, current, and PFC activation signal at full converter load.

8.EXPERIMENTAL RESULTS

After the completion of the driver, the controller, and the power parts of the designed system, the controller was loaded with the developed firmware by using Code Composer Studio (CSS) from Texas Instruments. The experimental setup is shown in Fig. 20, while Fig. 21. Shows the completely assembled PFC converter with driver and controller cards installed. After installing the system for experimental results as shown in Fig. 20, the first step is used to delay the start of the PFC controller. As expected, the input AC current waveform shown in Fig. 22 (blue) before the PFC starting is noticed to have a poor power factor. This is due to the operation of a regular rectifier (i.e., full wave diode rectifier formed by the built-in free-wheeling diodes of Si-MOSFETS and pre-charging diode bridge, BR1 in Fig. 13). After the PFC controller starts regulating the AC input current, the waveform of AC input current is shown in Fig. 22. The THD of the input current is measured to be 110% before without PFC function. With the PFC function, the THD of AC input current is measured using samples collected from ADC (Analog to Digital Converter) at 100 KSPS (Kilo Samples Per Second) and sending them back

the collected samples by the MCU to the PC over the virtual serial link provided by the implemented USB programmer/debugger. The collected samples are then processed by a MATLAB program to compute the THD. The AC input current with PFC mode at full rated power (3 kW) was 2.89% at 218 VAC input voltage and 400 VDC output. The load of the system is an electric heater that is modified by inserting tabs into the heater element for changing the load as required. The output voltage ripple has shown a 6Vpp at 1 kW load, while a 9Vpp DC output voltage ripple is recorded at 3 kW. Fig. 23 shows the output DC voltage at 1 kW load, 3kW load, and the voltage after turning off the PFC function. The power factor of the system is tested for different input voltages and various load steps. Fig. 24 Shows the system power factor for these test parameters.

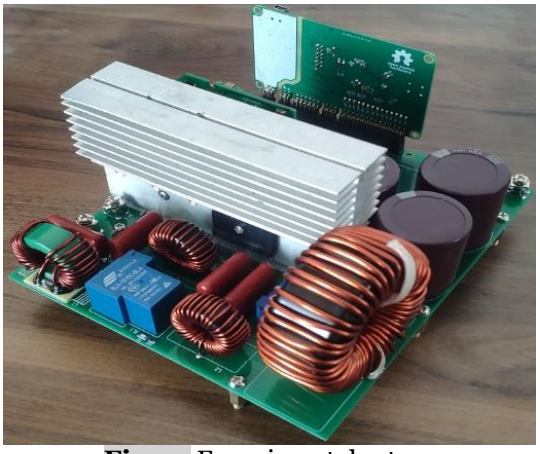


Fig.20 Experimental setup.

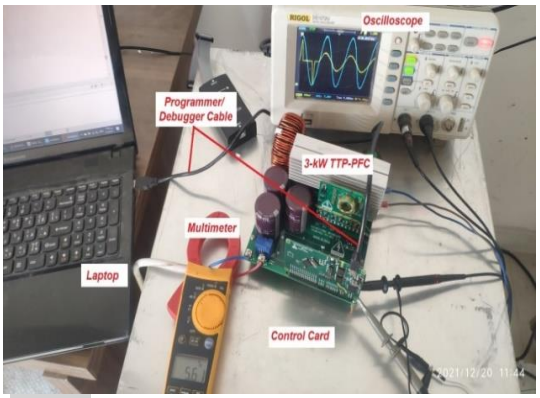


Fig.21 Final assembled system of 3 kW PFC converter.

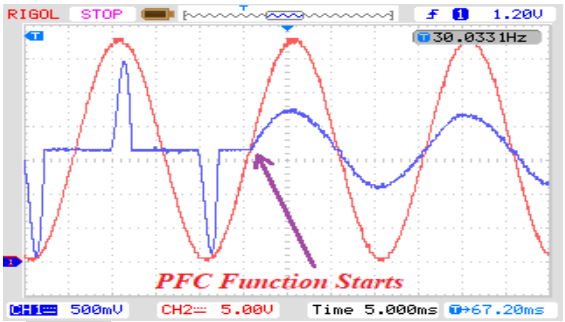


Fig.22 PFC function activation at full load.

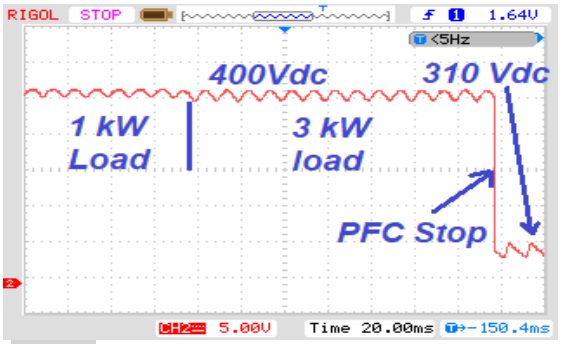


Fig.23 DC output voltage during 1 kW load, 3 kW load, and turning off the PFC.

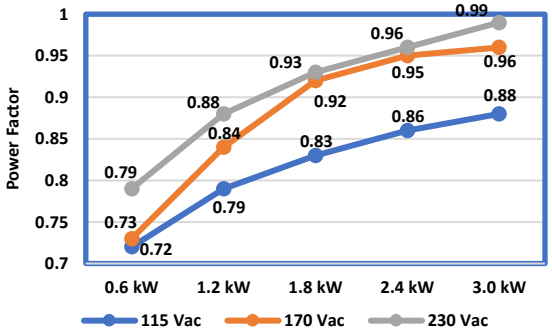


Fig.24 Power factor for various AC input voltages versus output power.

9.CONCLUSION

In this paper, a detailed design and implementation for a 3 kW totem pole PFC converter were presented. The design is based on GaN MOSFETs for high-frequency switches has been adopted, while two regular Si-based MOSFETs have been used and switched at line frequency. This configuration has led to a great reduction in system losses and hence, high efficiency (98.6%) was achieved. This design also proposed a configuration for converting the controller PWM output of regular PFC converters based on single switch topologies to be used in this totem-pole configuration. This modification is very useful for using the readily available single-PWM output analog PFC controller IC's and converting them into totem-pole controllers. The use of modern MCU with powerful CPU processing has enabled the use of a fast (100 kHz) current loop for better controller current tracking of reference input AC voltage leading to a near-unity power factor (0.99 has been achieved at full rated power).

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