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Article

Evaluate the Effect of a High-k Gate Dielectric on MOSFET Performance Using Silvaco TCAD Simulation

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Abstract:

One of the significant problems with MOSFET scaling down is oxide breakdown and tunneling current. One way to address this problem is to adopt silicon-based MOSFETs with high-k dielectric materials in their gates that work well as substitutes for traditional SiO_2 gates. Because high-k oxides reduce leakage and boost efficiency, these MOSFET variations can be used in low-power and high-performance applications. In the current work, the performance of the MOSFET device was studied by simulation utilizing different high-k materials, such as Si_3N_4, HfO_2, Al_2O_3, and TiO_2, as substitutes for the traditional SiO_2 gate insulator layer. SILVACO TCAD software simulator was used to simulate the MOSFET devices for different channel lengths and gate thicknesses. The dimensions of the channel lengths with corresponding gate insulator thickness were 100 nm, 3 nm, 50 nm, 1.2 nm, and 25 nm, 0.6 nm. The simulation delved into the impacts of different configurations in device design by analyzing electrical attributes like drain current, leakage current, threshold voltage, and current ratio. The results revealed that using high k-materials with the same physical oxide thickness improved switching speed and decreased sub-threshold voltage. When the channel length and oxide thickness scaled to 1.4, an enhancement in the switching speed and stability in threshold voltage were obtained by increasing the dielectric constant of the gate oxide layer. Further reduction in the channel length and oxide layer thickness gave undesirable results.

Keywords:

High-k materials; Insulator thickness; MOSFET Gate material; Threshold voltage; SILVACO TCAD.

Highlights:

- Replacing the MOSFET traditional gate insulator with high-k dielectrics offers a solution for scaling down issues.
- The suggested high-k dielectric materials are Si3N4, HfO2, Al2O3, and TiO2.
- Silvaco TCAD was used in the MOSFET device simulation.

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1.INTRODUCTION

It is more than two decades since the technology has controlled the process of diminishing the size of MOSFET devices [1, 2]. It seems that the device's scale-down will continue for years as it is led to reduce the cost. Due to Moore's law-driven device scaling, MOSFET devices required certain improvements, which might be achieved by introducing new materials or implementing new designs for new devices. As a result of scaling down, MOSFETs show degradation in performance in a variety of applications when the device channel length is scaled below 32 nm because of Short Channel Effects (SCEs), such as punch through, Gate Induced Drain Leakage (GIDL) and Drain Induced Barrier Lowering (DIBL) [3, 4]. The microelectronics industry has used silicon dioxide (SiO_2) as a dielectric material for the last three decades. With the fast advancement of integrated circuit and transistor technology, the gate oxide thickness has been steadily reduced daily. Recently, gate oxide has been effectively reduced in thickness up to 2 nm [5]. However, if SiO_2 thickness scales get less than 2 nm, tunneling-related leakage currents will significantly rise and thus negatively impact device reliability, which results in unfavorably high power consumption [6]. Consequently, to counteract this, the gate capacitance should be increased by substituting a high-k material instead of SiO_2. High-k-value metal oxide materials that can be involved in the MOSFET manufacturing process have recently been the focus of many studies. Al_2O_3, HfO_2, and TiO_2 are only a few of the high-k compounds currently being researched [7]. These materials are selected within certain constraints, including dynamic stability with the silicon layer (substrate), thermal stability, a sufficiently high dielectric constant, and a large band offset [8]. Within high-k materials, certain ones are compatible well with silicon, while others possess either excessively low or high dielectric constants, rendering them potentially unsuitable for deployment as alternative gate dielectrics. To increase efficiency and minimize short channel effects, high-k dielectric materials must be used in the MOSFET device's short channel length. The current MOSFET device simulation research focuses on designing a MOSFET using high k dielectric materials substitute to the conventional gate oxide layer (SiO_2). Such dielectric materials with high-k have decreased direct tunneling gate leakage current in MOSFET technology. We have a variety of high-k dielectric materials that are promising in terms of mobility, electrical conductivity, and thermal conductivity. This paper investigates the use of high-k dielectric materials and their impact on MOSFET performance with different channel lengths, including I-V characteristic, electric field, gate capacitance, threshold voltage, V_{th}, drain current, I_{on}, leakage current, I_{off}, and transconductance, g_m. The following parts show the characterization of the paper: The properties of high-k materials and MOSFET device structure are described in section 2, in which all relevant parameters have been taken, and simulation conditions are used in MOSFETs. The simulation results for the MOSFETs device are described in section 3. This section shows the DC analysis of MOSFETs' performances and a comparison with standard MOSFET devices. Section 4 describes the conclusion of the work based on the simulation results.

2.DEVICE STRUCTURE

2.1.Properties of High-k Materials

In general, high-k materials are materials that have a dielectric constant greater than 9, which refers to a group of elements in bilateral and triplex form of metal oxide, including transition elements of group III to group V, the aluminum and lanthanides [9]. Direct tunneling has a clearer effect at a gate oxide thickness of 40 Å or less. The high current flow through the gate dielectric will confine the device's accuracy [8], so a lower leakage current is needed to keep the device's reliability. Therefore, thicker gate oxide thickness is a necessity. To keep gate capacitance without curtailment of the SiO_2 thickness, a high-k material is required. Many researchers have provided several high-k materials such as Al_2O_3, Si_3N_4, ZrO_2, HfO_2, mixtures of high-k material, or metal oxide compounds [10]. Some limitations need to be met when choosing high-k materials, followed by the International Technology Roadmap for Semiconductors (ITRS) to replace the conventional dielectric material (SiO_2) [11]. These limitations include (i) dynamic stability with the silicon layer (substrate), (ii) thermal stability, (iii) a sufficiently high dielectric constant, and (iv) large band offset.

The gate capacitance is the heart of the MOSFET since the MOSFET is considered a capacitance-operated device; also, as the dielectric constant increases (k), the gate capacitance increases. Eq. (1) [3] illustrates how to calculate the C_{ox}.

$$\frac{C_{ox}}{A} = \frac{k \times \varepsilon_0}{t_{ox}} \qquad \textbf{(1)}$$

Where A is the area of capacitance, t_{ox} is the gate oxide thickness, ε_0 is the permittivity of free space $\varepsilon_0 = 8.85 \times 10^{-12}$ C^2/Nm^2, k is the dielectric constant. As the C_{ox} increases, the drain current increases. Eq. (2) [11] shows the relation between the k, C_{ox}, and I_{on}.

$$I_d = \frac{1}{2}\mu\, C_{ox} \frac{W}{L} (V_g - V_{th})^2 \qquad \textbf{(2)}$$

where I_d is a drain current, μ is the surface mobility of the channel, W and L represent the effective width channel and effective length channel, V_g is the gate voltage, and V_{th} is the threshold voltage.

It is possible to keep the same gate capacitance value equivalent to the gate capacitance used by SiO_2 as an oxide by using a high-k material to maintain the same equivalent oxide thickness (EOT). The EOT is given by Eq. (3) [11].

$$EOT = t_{high\_k}\frac{k_{SiO2}}{k_{high\_k}} \qquad (3)$$

Where t_{high_k} is the physical thickness of a high-k material, and k represents a dielectric constant.

2.2.MOSFET Device Structure

Different structures of the MOSFET were simulated using the SILVACO TCAD tool. The first model (standard model) used a gate length of 100 nm and an oxide thickness of 3 nm [12]. A variety of high *k* materials were used individually as an alternative to the standard oxide layer to examine its impact on the MOSFET performance. The alternative chosen materials were Si_3N_4, Al_2O_3, HfO_2, and TiO_2, with dielectric constants (*k*) of 6.2, 9, 25, and 80, respectively. During the use of these different dielectric materials, the gate contact material was kept constant with a work function of 4.6 eV. For all the structures under study, the source and drain were doped by uniform concentration donor $N_D = 10^{20}$ cm^{-3} [12]. Table 1 summarizes the properties of MOSFET device characteristics. To explore the I-V characteristic, which focuses on threshold voltage, V_{th}, drive current, I_{on}, and leakage current, I_{off}, the oxide layer thickness, t_{ox}, and channel length, L_g, were varied. To find out which MOSFET structure performed better, their performances were compared. The channel length scaled down to 50 and 25 nm with oxide layer thicknesses of 1.2 nm and 0.6 nm, respectively. Each structure was examined separately. Fig. 1 illustrates the general structure of MOSFET under the study. The Si substrate was doped with acceptor impurities $N_A = 10^{17}$ cm^{-3}, and the contact metal on the source and drain was Al.

Table 1 Device Parameter Used for Simulation.

Parameters	Value
Source/drain doping	10^{20} cm^{-3}
Channel doping	10^{17} cm^{-3}
Oxide thickness	(3 nm, 1.2 nm, 0.6 nm)
Channel length	(100 nm, 50 nm, 25 nm)
Gate metalwork function	4.6 eV

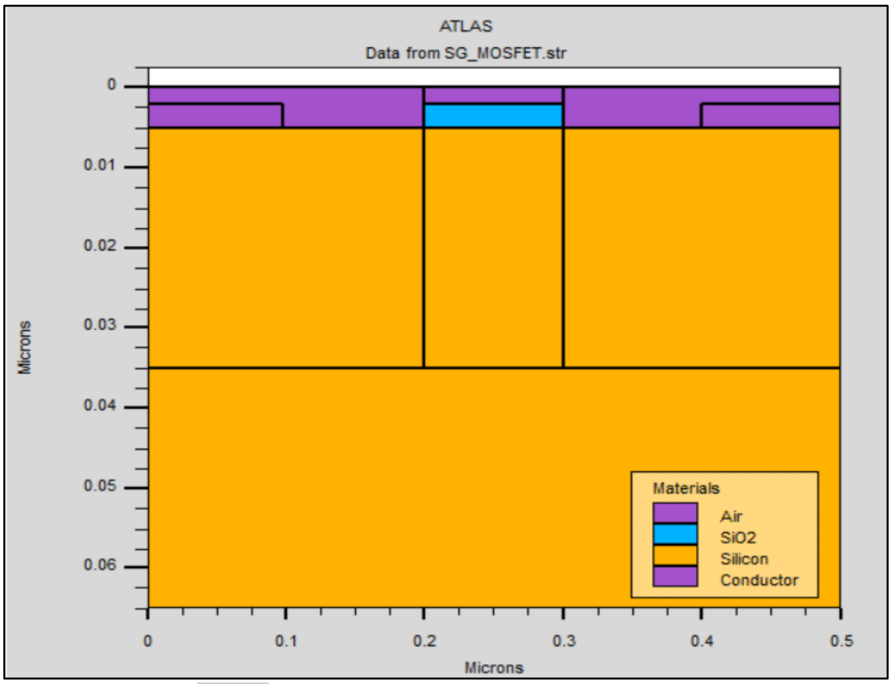


Fig. 1 General Device Layout of MOSFET.

3.RESULTS AND DISCUSSION

Fig. 2 shows the electrical characteristic simulation results (I_d-V_g) for the MOSFET with SiO_2 as a gate dielectric material. The extracted MOSFET parameters from Fig. 2, I_{on}, I_{off}, V_{th}, and g_m are 0.3 mA, 5.77 pA, 0.606 V, and 0.85 mS, respectively. Because many high-k materials have superior thermal stability and lower interface state density than SiO_2 [13], it is necessary to investigate the impact of some of these materials on the MOSFET performance by keeping the oxide capacitance constant. This is achieved by using the same equivalent oxide thickness EOT. According to Eq. (3) [14], the physical thickness of the alternative gate oxide materials is thicker than the thickness of the SiO_2 by a factor of k_{high_k}/k_{SiO2} [15]. The different gate oxide materials were Si_3N_4 (k=6.2), AL_2O_3 (k =9), HfO_2 (k =25), and TiO_2 (k =80), with physical thicknesses of 4.76 nm, 6.9 nm, 19.2 nm, and 61.53 nm, respectively. Fig. 3 illustrates the I_d-V_g curve for different high-*k* materials. Table 2 summarizes the electrical parameters extracted from Fig. 3.

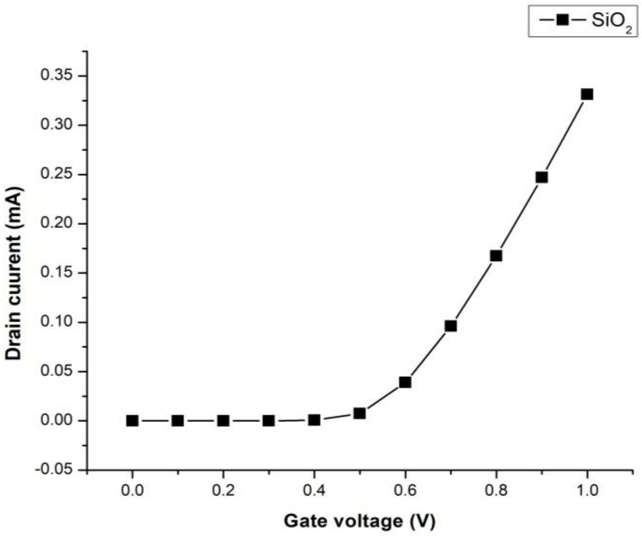


Fig. 2 Drain Current I_{on} for MOSFET with SiO_2 as Gate Dielectric, L_g=100nm, and t_{ox}=3nm.

It is shown that the permittivity of dielectric materials determines the I_{on} of those materials in proportion. It is observed that the I_{on} value increases when a higher permittivity of high-*k* dielectrics is utilized as the gate insulator, where TiO_2 has a larger value of I_{on} ~0.39 mA. It can be noticed that even the I_{on} increases with the *k* value of the insulator layer, but at the same time, I_{Off} will also increase, especially at *k*>25. The rate at which a transistor can be turned on or off is indicated by its sub-threshold slope. A transistor that slowly changes from an off to an on state is indicated by a large sub-threshold voltage [16]. The results of V_{th} reveal that, for the fixed oxide thickness, the increase in the dielectric constant of the insulator layer produces a slight enhancement in the threshold voltage. To investigate the impact of the electrical field distribution for various gate insulator materials on the source and drain regions through the gate insulator, Fig. 4 (a) to (d) are presented. It can be noticed with an increase in the *k* value, the electric field lines intensify from the gate towards the source and drain regions, and this appears very clearly at *k* =80. This lowers the channel barrier potential and causes short-channel effects, which makes the gate's ability to control the channel less effective [17-18]. From the aforementioned, it can be deduced that increasing the physical thickness by increasing the dielectric constant for the same EOT hurts the performance of the MOSFET due to the degradation of electrostatics. Consequently, the thick oxide layer reduces the gate's control over the channel. Therefore, it is necessary to study the impact of high−*k* gate dielectric material by keeping the same physical thickness of the insulator.

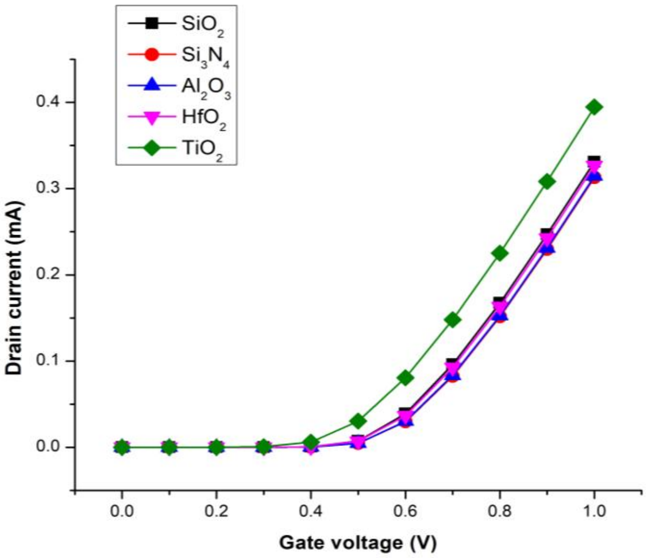
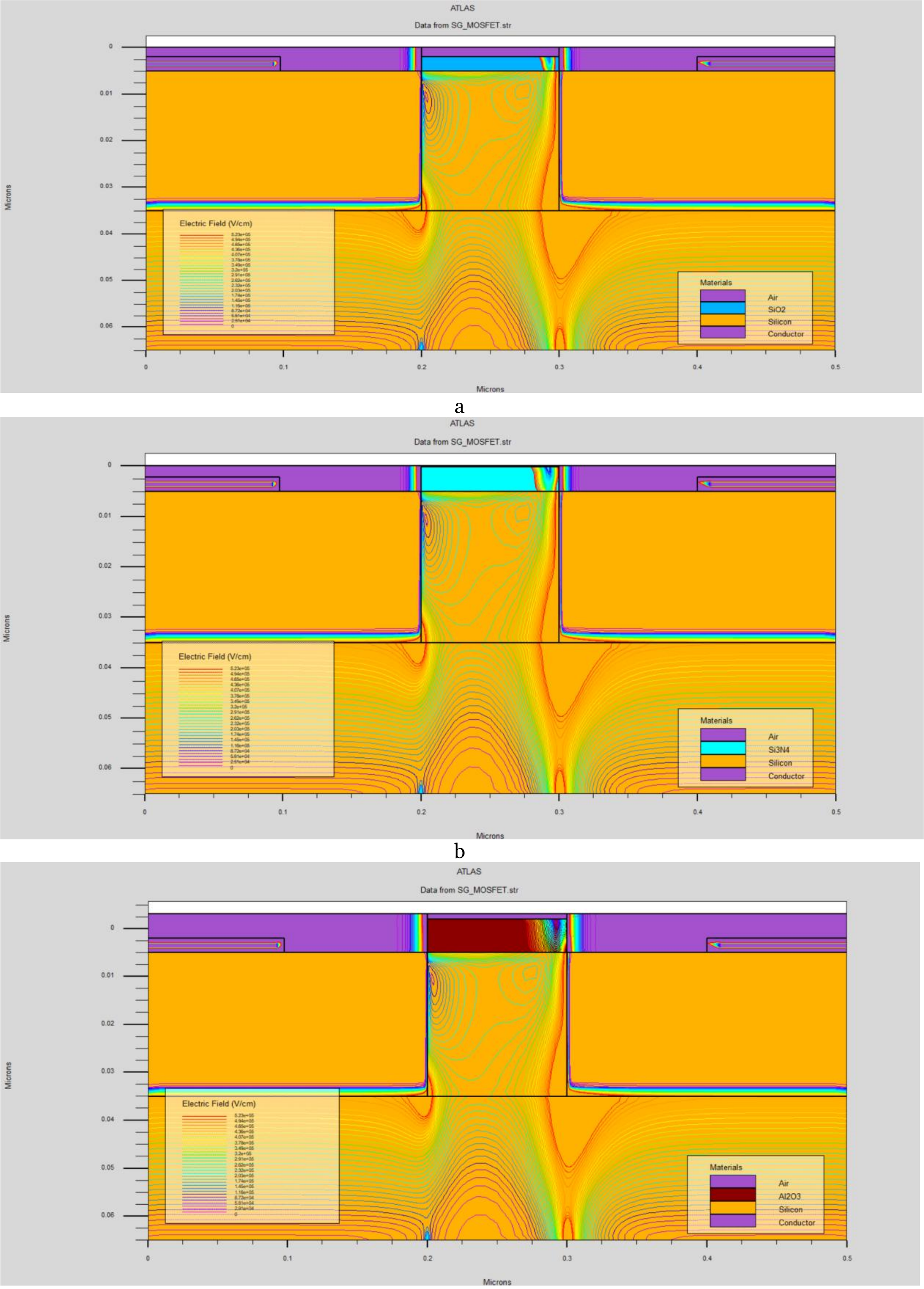


Fig. 3 Behavior of Drain Current (I_{on}) as a Function of Gate Voltage (V_g) at V_{ds}=1V for different High k-Materials with the Same EOT.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2.03e+05
1.74e+05
1.45e+05
1.16e+05
8.72e+04
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Silicon
Conductor
Si3N4
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a

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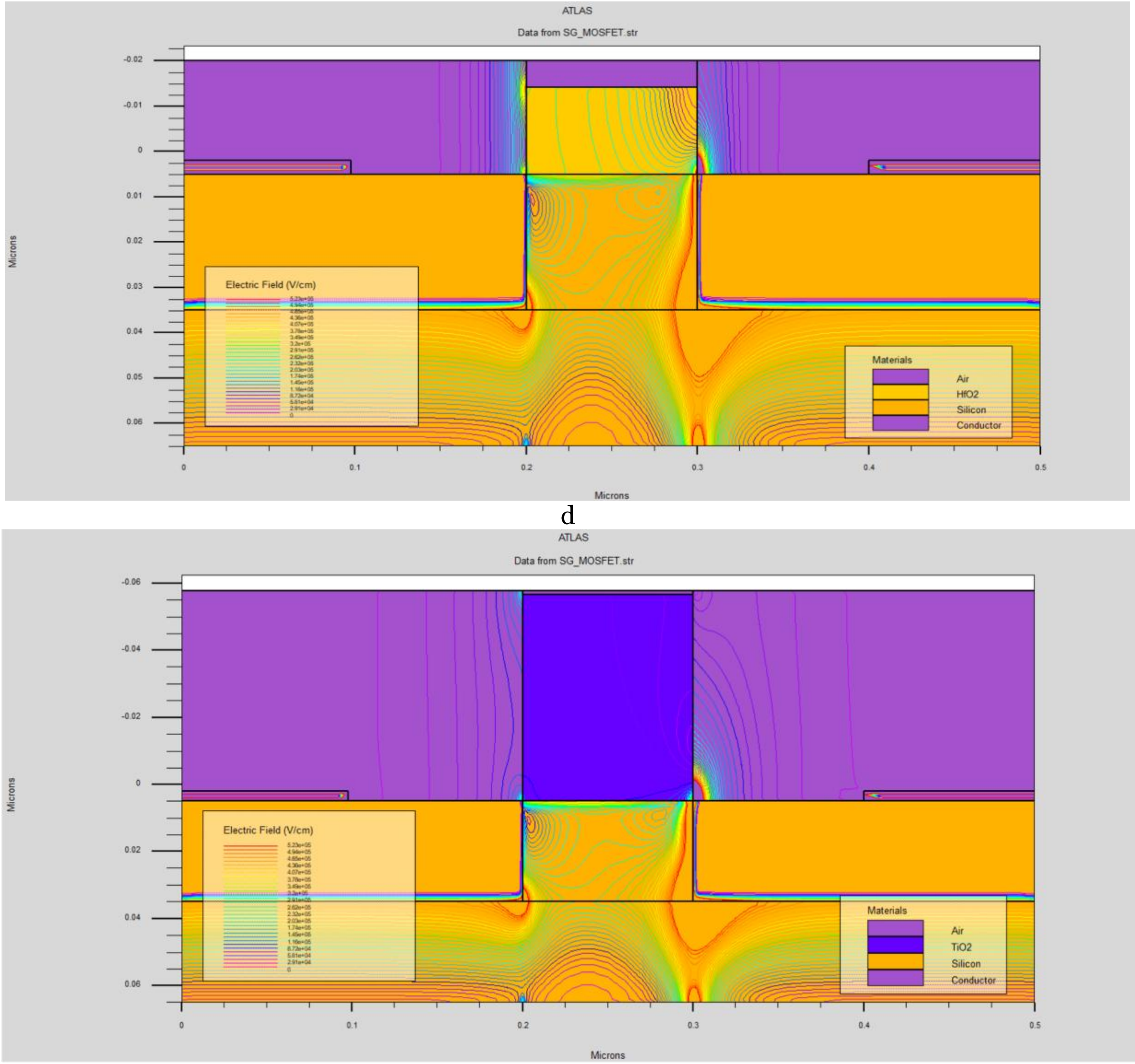


d

e

Fig. 4 Behavior of Electric Field for different High k-Materials Keeping EOT = 3 nm in Each Case for (a) SiO_2 with t_{high_k}=3 nm (b) Si_3N_4 with t_{high_k} =4.76 nm (c) Al_2O_3 with t_{high_k}=6.9 nm (d)HfO_2 with t_{high_k}=19.2 nm (e) TiO_2 with t_{high_k}=61.53 nm.

Table 2 Electrical Characteristics of MOSFET by Using different high-k Materials with the Same Equivalent Oxide Thickness (EOT=3 nm).

parameter	I_{on} (mA)	I_{off} (pA)	V_{th} (V)	I_{on}/I_{off} 10^7	SS (mV/dec)
SiO_2	0.30	5.72	0.606	5.7	79
Si_3N_4	0.31	2.63	0.62	11.8	78
Al_2O_3	0.31	2.86	0.62	10.9	78
HfO_2	0.32	7.49	0.61	4.3	81
TiO_2	0.39	340	0.54	0.115	90.9

3.1.Effect of a High-k Material on the MOSFET Performance with the Same Physical Thickness (thigh-k = 3 nm)

For given MOSFET dimensions, one of the methods used to increase I_{on} is increasing C_{ox}, and this can be achieved by using high dielectric materials in the gate oxide layer while keeping the oxide layer thickness constant. For this purpose, in the present simulation, the physical thickness of the gate oxide layer was fixed at 3 nm. As the dielectric constant (k) increased, the gate oxide capacitance C_{ox} increased, which reflected positively on the value of I_{on}. On the contrary, the gate oxide capacitance C_{ox} is proportional inversely to the short channel parameter SS [19]. The device's I_{on}/I_{off} ratio, which is crucial for its low power consumption and digital logic application, is also improved by enhancing SS. Similar to the SS, V_{th} is also proportional inversely with the gate oxide capacitance [20]. Enhancing V_{th}, which is dependent on channel and oxide materials once more, can influence DIBL. Therefore, manipulating the gate oxide layer property, i.e., dielectric constant, is crucial for improving the MOSFET performance.

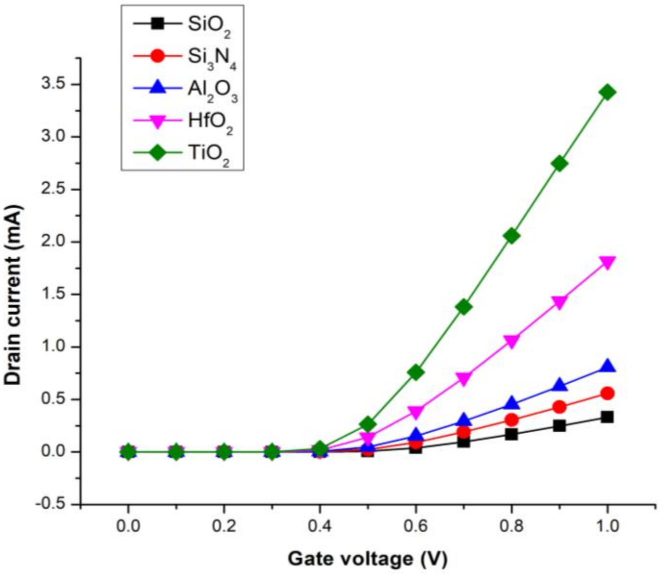


Fig. 5 Behavior of Drain Current (I_{on}) as a function of Gate Voltage (V_g) for different high *k*-materials at V_{ds}=1 V Lg=100 nm, and $t_{high\text{-}k}$=3 nm.

Figure 5 shows the I_d-V_g characteristics plot for the MOSFET for different high *k*- materials as a gate oxide layer at constant V_{ds} =1 V. It can be seen how the main MOSFET performance parameters, i.e., the threshold voltage (V_{th}), state on current (I_{on}) and state off current (I_{off}), were affected by using different high *k* materials as a gate oxide layer. The extract results are summarized in Table 3. It is observed from the data in Table 3 that there is an enhancement in the I_{on} and an uptick in I_{off} with increasing the dielectric constant of the oxide layer. It is worth mentioning that the values of leakage current in the range of *pA* can be considered unaffected when using high *k* materials as a gate oxide layer. In general, there was a heightening in the I_{on}/I_{off} ratio. In the same context, the high *k* dielectric constant of the gate oxide layer produced a low threshold voltage and a reduction in the value of the sub-threshold slope, reflecting the speed of the MOSFET device. Replacing SiO_2 with a high *k*-material resulted a high value of surface potential, thus increasing the inversion charge density. This increase in surface potential thereby the reduction in the device threshold voltage, and an increase in carrier density led to a rise in device field effect mobility [21]. The SS characteristics showed that the value of the sub-threshold slope was lower when a higher dielectric constant was used, and this can be ascribed to an increase in the gate capacitance, as shown in Table 3 [22]. All the dielectric materials produce a nearly ideal SS in the range of 60 to 70 mV/dec.

Table 3 Electrical Characteristics of MOSFET by Using different high-k Materials with the Same Physical Oxide Thickness ($t_{high\text{-}k}$ = 3 nm).

Parameter	I_{on} (mA)	I_{off} (pA)	V_{th} (V)	I_{on}/I_{off} 10^7	SS (mV/dec)	Cg (fF/µm)
SiO_2	0.3	5.72	0.606	5.7	79	0.8
Si_3N_4	0.5	8.18	0.569	6.82	72	1.27
Al_2O_3	0.8	10.6	0.55	7.57	69	1.79
HfO_2	1.81	17.5	0.523	10.3	65	4.03
TiO_2	3.42	22.2	0.501	15.4	63	8.31

3.2.Effect of a High-k Material on the MOSFET Performance with Dimensions Scaled Down

Since the new technologies concentrated on reducing the production cost and, at the same time, producing large quantities of MOSFET, the size of gate length (L_g) was targeted to reduce its length from hundreds *nm* to tens *nm* scale. The MOSFET scaling down produces various short-channel effects (SCEs). As the channel length decreases, the drain and source share more of the charge, and the gate's control over the channel region is lost. The threshold voltage is reduced as a result. The primary focus of MOSFET research over the past few decades has been developing new strategies to mitigate short-channel effects. Numerous researchers have offered numerous ways to lower these SCEs [21, 23, 24]. Reducing the effective thickness of gate oxide while maintaining the same physical thickness through different methods is one of the effective options. So, the second part of the current study focused on the impact of using high k dielectric materials as a gate insulator layer under MOSFET channel length scaling down conditions. The channel length was scaled down to 50 nm and 25 nm with a reduction in the thickness of the oxide layer by 1.2 nm and 0.6 nm, respectively. Fig. 6 shows the transfer characteristics of the MOSFET with different dielectric materials as gate insulator layers of a 50 nm channel length and 1.2 nm oxide thickness. It is evident that the highest current transfer characteristic belongs to TiO_2, followed by HfO_2, Al_2O_3, Si_3N_4, and SiO_2. It is clear from the graph that using high-*k* dielectrics can enhance the transfer characteristic. The calculated characteristics of the MOSFET, i.e., I_{on} and I_{off} and sub-threshold, were extracted from Fig. 6 and listed in Table 4. The results showed an enhancement in the I_{on}, which increased from 1.26 mA to 3.4 mA when the SiO_2 was replaced by TiO_2 as a gate insulator material. In the same vein, the results revealed a reduction in the I_{off} by using a high *k* material as a gate insulator layer, which represented a drop in the leakage current where it decreased from 2.45 μA to 0.674 μA for SiO_2 and TiO_2 as insulator layer respectively. As a result, a boost in the I_{on} to I_{off} ratio was obtained. It is worth to note that, with the reduction in the channel length, there was no noticeable impact of using high *k* material on the V_{th} where its value ~0.4 V, as shown in Table 4. It is worth noting that with channel length reduction, a deterioration in the value of SS was obtained, where its values ranged from 219 mV/dec for SiO_2 to 146 mV/dec for TiO_2. Although the high *k* material produced a low SS value, it is still higher than the optimum value. The increase in the SS values can be ascribed to a rise in the slope factor (*n*) for ($\log I_d$ vs V_d), which is impacted by the gate capacitance, as shown in Table 4 [22]. By comparing the results obtained for the case of L_g = 50 nm with the previous case of the Lg =100 nm for the corresponding insulator materials, one can notice that the reduction in gate length produces large values of I_{on} and I_{off} and a drop in the values of V_{th}. It is observed from the data in Table 4 that there is an enhancement in the I_{on} and a decrease in I_{off} with increasing the dielectric constant of the oxide layer, while the threshold voltage is almost unaffected by the oxide layer dielectric constant.

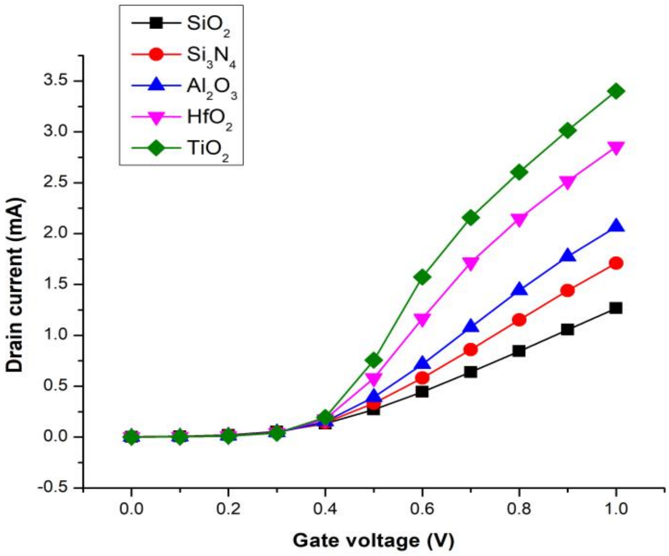


Fig. 6 Behavior of Drain Current (I_{on}) as a function of Gate Voltage (V_g) for different high k-materials at V_{ds}=1 V, Lg=50 nm, and $t_{high\text{-}k}$=1.2 nm.

Table 4 Electrical Characteristics of MOSFET by Using different High-k Materials with the Same Equivalent Oxide Thickness ($t_{high\text{-}k}$ = 1.2 nm) and Channel Length of 50 nm.

Parameter	I_{on} (mA)	I_{off} (μA)	V_{th} (V)	I_{on}/I_{off}	SS (mV/dec)	C_g (fF/μm)
SiO_2	1.26	2.45	0.402	517	219	0.90
Si_3N_4	1.71	1.56	0.406	1090	200	1.3
Al_2O_3	2.06	1.2	0.402	1712	188	1.68
HfO_2	2.85	0.802	0.408	3558	159	2.88
TiO_2	3.4	0.674	0.407	5042	146	3.54

For a comprehensive investigation of the impact of using a high *k*-dielectric material as a gate insulator layer, the dimension of the channel and insulator layer for the last MOSFET structure was scaled down by a factor of 1.4 to reach the gate length and gate dielectric thickness of 25 nm and 0.6 nm, respectively. While the doping of each part of the device was kept at the same previous concentration. The transfer characteristics of the MOSFET for the channel scale-down and different high materials are shown in Fig. 7, and the extracted characteristics are summarized in Table 5. Although the results of the scaled-down structure revealed an enhancement in the threshold voltage where it decreased to a few hundred of mV (about 50% less than the previous case), an undesirable increase in the

I_{off} was obtained, which produced a reduction in the I_{on}/I_{off} ratio. Even though using high k materials, the value of I_{off} was still very high relative to the aforementioned cases of longer channel dimension. To explain the huge increase in the I_{off} with channel dimension reduction, we looked at electric field behavior for different gate high-k insulator materials. Fig. 8 (a) to (e) reveals the electric field distribution along the device channel. It is evident that a higher gate fringing field results from increasing the k of insulator material and this reduces gate control in sub-micron MOSFETs. This degrades the short-channel effects and reduces the MOSFET threshold voltage for higher $t_{high\text{-}k}$ / L levels [25].

Table 5 Electrical Characteristics of MOSFET by Using different High-k Materials with the Same Equivalent Oxide Thickness ($t_{high\text{-}k}$ = 0.6 nm) and Channel Length of 25 nm.

Parameter	**I_{on} (mA)**	**I_{off} (μA)**	**V_{th} (V)**	**I_{on}/I_{off}**	**SS (mV/dec)**
SiO_2	2.7	667	0.12	4.13	1070
Si_3N_4	3.1	645	0.18	4.85	840
Al_2O_3	3.3	632	0.20	5.3	710
HfO_2	3.9	610	0.26	6.44	520
TiO_2	4.3	605	0.28	7.10	440

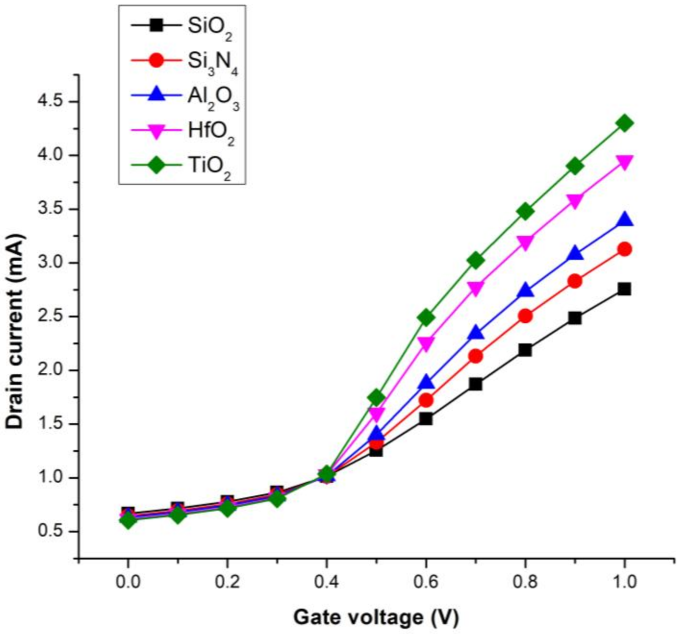
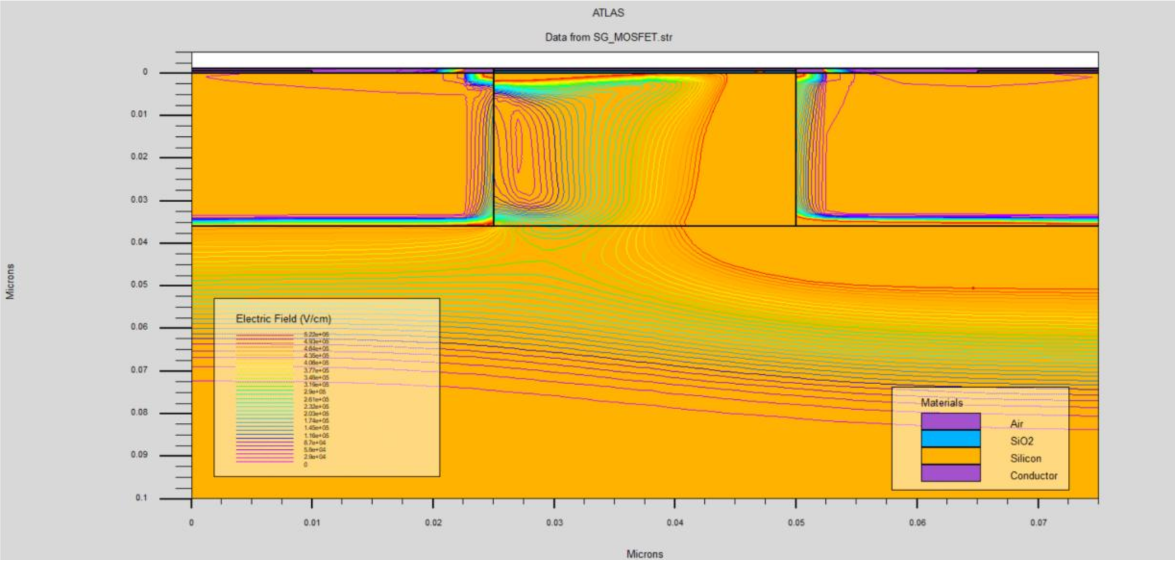


Fig. 7 Behavior of Drain Current (I_{on}) for different high k-materials at V_{ds} =1 V, Lg=25nm, and $t_{high\text{-}k}$=0.6.



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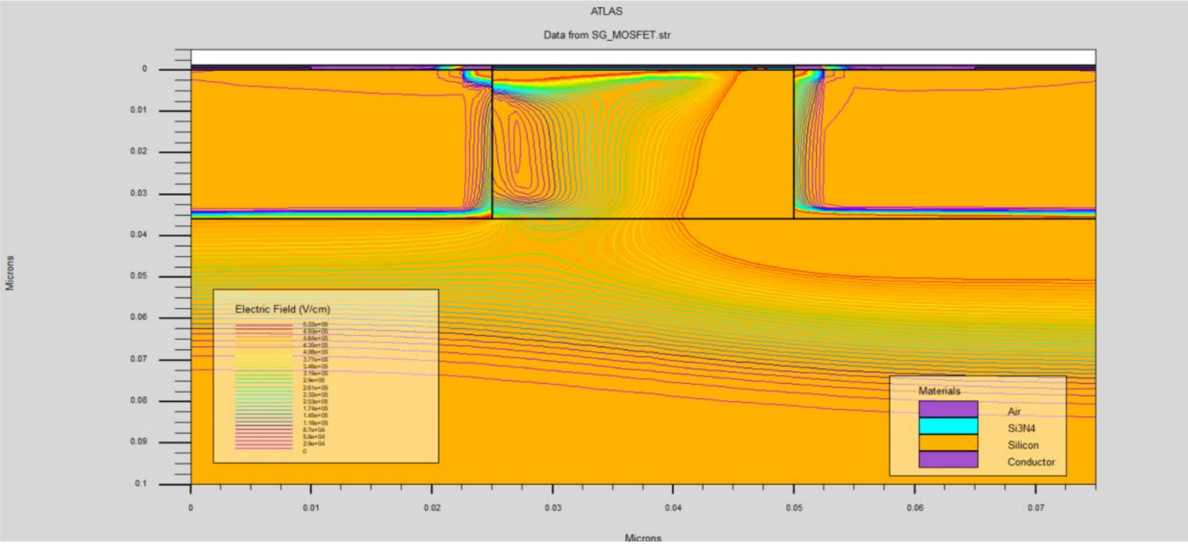
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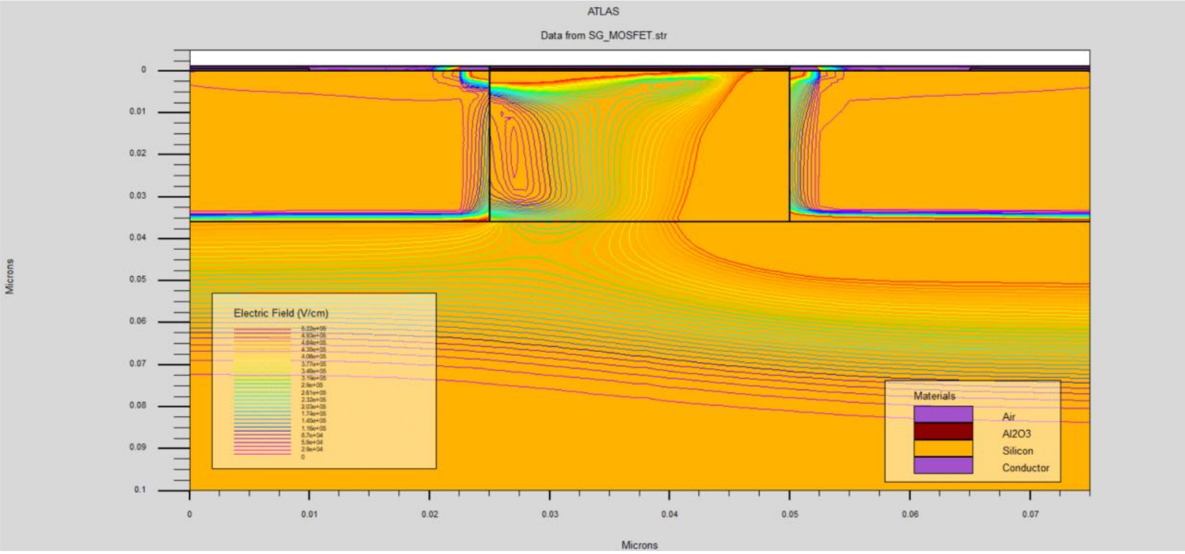
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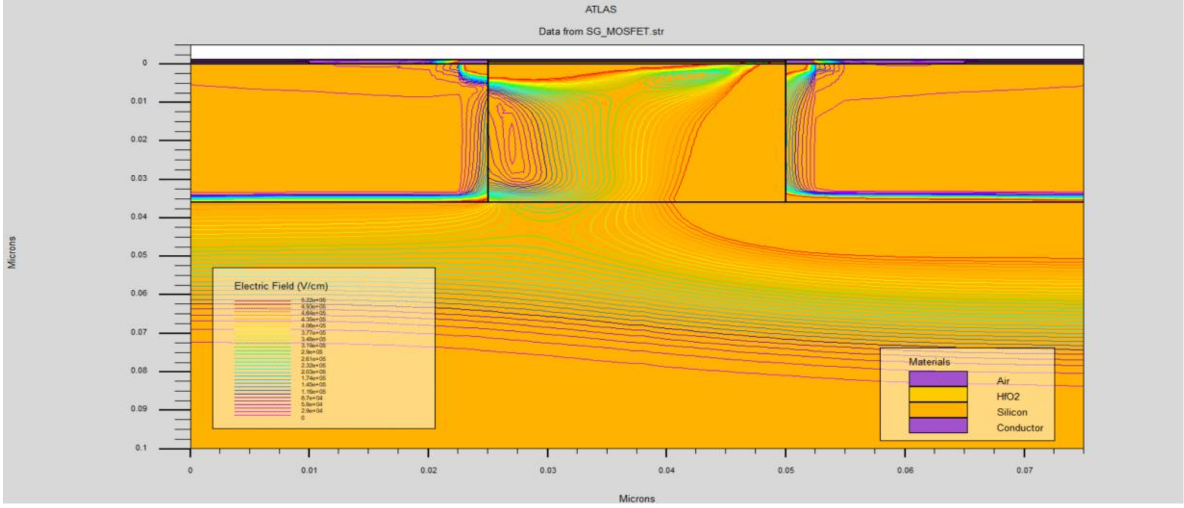
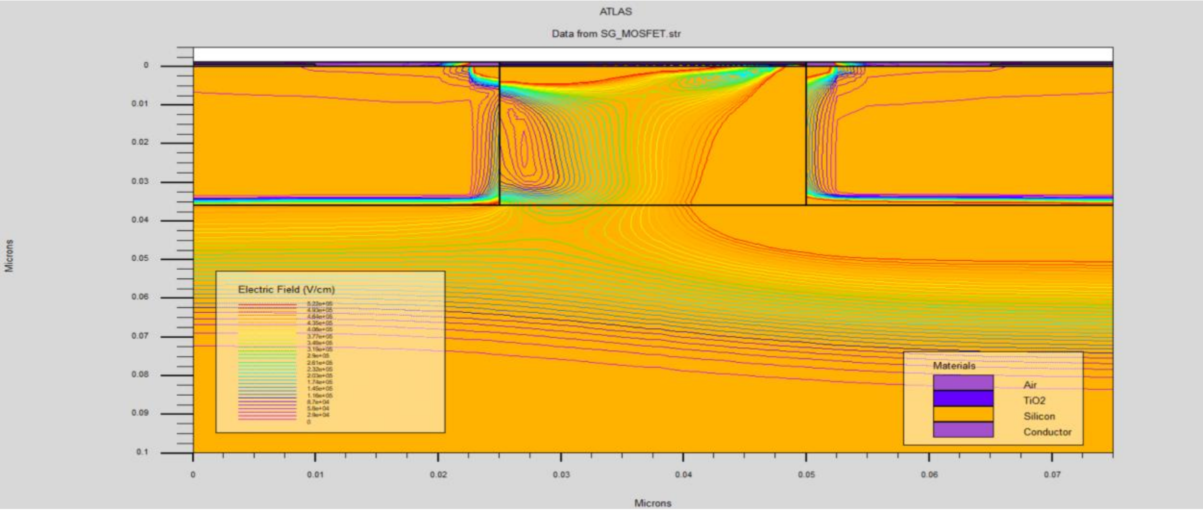
0.05
0.06
0.07
0.08
0.09
0.1
Electric Field (V/cm)
5.22e+05
4.93e+05
4.64e+05
4.35e+05
4.06e+05
3.77e+05
3.48e+05
3.19e+05
2.9e+05
2.61e+05
2.32e+05
2.03e+05
1.74e+05
1.45e+05
1.16e+05
8.7e+04
5.8e+04
2.9e+04
0
Materials
Air
Al2O3
Silicon
Conductor
0
0.01
0.02
0.03
0.04
0.05
0.06
0.07
Microns

c


ATLAS
Data from SG_MOSFET.str
Microns
0
0.01
0.02
0.03
0.04
0.05
0.06
0.07
0.08
0.09
0.1
Electric Field (V/cm)
5.22e+05
4.93e+05
4.64e+05
4.35e+05
4.06e+05
3.77e+05
3.48e+05
3.19e+05
2.9e+05
2.61e+05
2.32e+05
2.03e+05
1.74e+05
1.45e+05
1.16e+05
8.7e+04
5.8e+04
2.9e+04
0
Materials
Air
HfO2
Silicon
Conductor
0
0.01
0.02
0.03
0.04
0.05
0.06
0.07
Microns

d



e

Fig. 8 Electric Field Distribution at Channel Length=25nm and $t_{high-k} = 0.6\ nm$ for (a) SiO_2 (b) Si_3N_4 (c) Al_2O_3 (d)HfO_2 (e) TiO_2.

4.CONCLUSIONS

A high k-materials, namely Si_3N_4, Al_2O_3, HfO_2, and TiO_2, were used to compare the MOSFET device's performance in terms of the I-V characteristic, electric field, gate capacitance, threshold voltage, V_{th}, drain current, I_{on}, leakage current, I_{off}, and transconductance. The comparison was conducted under scaling conditions ranging from 3 nanometers and 100 nanometers down to 0.6 nm and 25 nm, respectively, for gate oxide thickness and channel length. Despite the improvement obtained by utilizing high dielectric constant materials, the device's performance declined in terms of leakage current, I_{off}, and subthreshold swung, SS when scaling down the dimension of the device. In particular, when high-k dielectric materials were utilized, the leakage current was reduced and the drain current (I_{on}) increased at 50 nm channel length and 1.2 nm oxide thickness. Moreover, it was noted that the device's SS decreased when high-k materials were used, while it was still greater than the ideal value. However, in terms of communication applications, this gadget may still compete. When the device dimensions were scaled down more by a factor of 1.4, an undesirable increase in leakage current, I_{off} was obtained, leading to a decrease in the ratio of I_{on}/I_{off}. Even with the use of high-k dielectric materials, the leakage current, I_{OFF} remained very high. This issue can be addressed by increasing the impurity ratio, type- p in the channel region of the MOSFET device. Also, it can improve the device performance by using stack gate engineering to confine the fringing field within the channel.

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