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Integrated Single Stage Power Amplifier Based GaAs FET with Filter for Bluetooth Applications

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Keywords:
ADS software; Bandpass filter; GaAs FET; Microstrip technology; Matching network (MN); Power amplifier.

Highlights:

- Integrated Single-Stage Power Amplifier Based on GaAs FET with Filter.
- A bandpass filter (BPF) was used as an output matching network, effectively reducing the size and power consumption of the power amplifier.
- Structural performance was performed using the Advance Design System tool.

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Abstract: This work presents the design, analysis, and simulation of a single-stage power amplifier integrated with a bandpass filter at 2.4 GHz. The embedded GaAs FET transistor, MGF2407A, in the Advanced Design System tool, is the heart of the amplifier circuit, operating in class AB mode at a drain-source voltage of 3.2 V and a gate-source voltage of -1.4 V. The source and load impedances have been extracted using the source and load-pull technique. Matching circuits were then designed and optimized at the input and output of the transistor. The simulated stability factor of the amplifier exceeded 3 in the frequency band from 2 to 3 GHz, with a maximum value of 4.27 at 2.4 GHz. The maximum simulated power gain and Power-Added Efficiency were 12.7 dB and 68.78%, respectively, at 2.4 GHz, with very low reflection coefficients at the input and output sides, with values below -23 dB. The amplifier was capable of delivering an output power of 5 dBm and 22 dBm at input power -10 dBm and 7 dBm, respectively, which meet the requirements of long-distance Bluetooth and long-term evolution applications. Simulation results also showed that the amplifier had a wide bandwidth of 100 MHz and an acceptable size area of 57 x 32 mm². The amplifier circuit model reported here can be used to design and fabricate different amplifier circuits for a range of applications.

دائرة مكبر إشارة ذو مرحلة واحدة باستخدام GaAs FET مع مرشح ترددي لتطبيقات البلوتوث

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الخلاصة

يقدم هذا العمل تقريرًا عن تصميم وتحليل ومحاكاة مكبر القدرة أحادي المرحلة المدمج مع مرشح تمرير النطاق عند تردد عمل ٢,٤ جيجا هرتز. يعتبر ترانزستور GaAs FET المسمى MGF٢٤٠٧A في برنامج ADS هو قلب دائرة مكبر القدرة التي تعمل في وضع الفئة AB عند جهد مصدر التصريف البالغ (٣,٢) فولت وجهد مصدر البوابة البالغ (١,٤-) فولت. وقد تم استخراج ممانعات المصدر والحمل باستخدام تقنية المصدر وسحب الحمل وتم بعد ذلك تصميم الدوائر المطابقة وتحسينها عند مدخلات ومخرجات الترانزستور. اظهرت النتائج ان عامل الاستقرارية للمكبر الذي تم محاكاته كان اعلى من ٣ في حزمة التردد ما بين ٢ الى ٣ جيجا هيرتز، وقيمته ٤,٢٧ عند التردد ٢,٤ جيجا هيرتز. الحد الأقصى لمحاكاة طاقة الخرج واكتساب الطاقة وكفاءة الطاقة المضافة هو ٢٢ ديسيبل و١٢,٧ ديسيبل و٦٨,٧٨٪ على التوالي عند ٢,٤ جيجا هرتز، مع معامل انعكاس منخفض جدًا أقل من (٢٣-) ديسيبل. كما ان المكبر له القدرة على توصيل قدرة اخراج ٥dBm و٢٢dBm عندما تكون قدرة الادخال - ١٠dBm و ٧dBm على التوالي، وهو ما يلبي متطلبات المسافة الطويلة لتقنية البلوتوث وتطبيقات الجيل الرابع لأنظمة الاتصالات. أظهرت نتائج المحاكاة أيضًا أن مكبر الصوت لديه عرض نطاق قدره ١٠٠ ميجا هرتز، ومساحة مقبولة تبلغ ٥٧ × ٣٢ ملم٢. يمكن استخدام نموذج دائرة مكبر الصوت المذكور هنا لتصميم وتصنيع دوائر مكبر صوت مختلفة في نطاق من التطبيقات.

الكلمات الدالة: برنامج ADS، مرشح تمرير النطاق، ترانزستور ثنائي المجال، تقنية Microstrip، دوائر الموائمة، مضخم الطاقة.

1.INTRODUCTION

Over the last two decades, there has been a rapid advancement in the design and analysis of electronic circuits, such as power amplifiers, filters, low-noise amplifiers, detectors, and oscillators, to meet the demand for fast and reliable communication systems, as well as the huge requirement for high-data-rate wireless systems. Besides the primary goal of improving the performance of communication devices, the ambition is to reduce cost, power dissipation, and the effective size of these components, allowing more devices to be packed into electronic chips. The 2.4-2.5 GHz frequency band has received considerable attention due to its use in various applications, including Wireless LAN, Bluetooth, Wi-Fi, and cordless phones [1]. The linearity of power amplifiers plays a crucial role in determining the overall performance of communication systems; therefore, considerable attention must be paid, and careful processes must be followed in the design and production of such devices [1-3]. Class A, Class B, or Class AB power amplifier configurations have been widely employed to mitigate the issue of linearity and thus enhance the circuit's performance [4, 5]. Another crucial figure of merit is the efficiency of amplifiers, which mainly affects the power consumption and battery life of portable devices. One way to enhance the performance of power amplifiers and increase their power-added efficiency (PAE) is by employing cost-effective and straightforward design techniques, such as optimizing passive components and minimizing passive element losses [4, 6, 7]. Class AB power amplifiers operate between half and full waveform cycles of the output signal and are capable of achieving (50-78) % efficiency [8]. This behavior requires the transistor to be biased between the cut-off region and the Q-point of the class A transistor. Several efforts have been made to design and fabricate different classes, such as F- and J-classes, to improve the efficiency of bandwidth multiband capabilities [9-11]. The key components in integrating power amplifier circuits are matching networks and filters since they are crucial in defining the overall performance of such circuits. In Ref. [12], a single-stage class-AB Power Amplifier based on GaAs-FET was designed and simulated to operate in the 2.45 GHz frequency band for ISM applications. A "T" matching technique was employed at the input and the output sides of the transistor to achieve a maximum power gain of 19.4 dB. However, the amplifier had a limited bandwidth and small k-factor of 100 MHz and 1.158, respectively. Moreover, the amplifier occupied a large size of 73.5 x 36 mm^2 Ref. [13] presents a high-power amplifier matched by a bandpass filter for Long-Term Evolution (LTE) applications. The power amplifier exhibited a good gain of 14.4 dB. However, a low PAE of 46.3% and a narrow bandwidth of 100 MHz were achieved. The obtained high gain came at the expense of a large circuit size of 90 × 70 mm^2. In the present work, a 2.4 GHz class-AB power amplifier integrated with a bandpass filter was first analyzed and then designed and modeled using the schematic and layout design embedded in the ADS platform from Keysight Technology. The utilized approach employed a bandpass filter (BPF) to act as an output-matching network, effectively reducing the size and power consumption of the power amplifier. The work also focuses on achieving high output power while blocking unwanted frequencies from the desired band. The studied amplifier can provide a power gain of 12.7 dB for a wide bandwidth of 100 MHz. More importantly, the circuit exhibited good power-added efficiency (PAE) and occupied a relatively small fabrication area. The proposed circuit

performances could compete with those of other reported works [12, 14, 15] and would be an excellent choice for exploitation in Bluetooth and LTE transmitter systems.

2.AMPLIFIER DESIGN PROCESS

In the present work, a class AB configuration was selected due to its ability to provide high linearity and power-added efficiency (PAE) higher than 70% [16], which are key requirements for Bluetooth applications, as depicted in Table 1. The simplified structure of the proposed power amplifier is shown in Fig. 1, which includes a filter, input and output match networks, and a single amplifying FET transistor. Both input and output matching networks are required to mitigate the mismatch between the transistor impedances and the input/output terminals, thereby increasing the amplifier's efficiency. A low-cost and available transistor was utilized in this work, named (MGF2407A) [17], embedded in the ADS library. The transistor can operate at a maximum frequency of 16 GHz and with a Vgs range of 0 to -4V. Moreover, the transistor can pump a drain current of up to 200 mA. However, it has a low stability factor (k) of less than 0.5 at 2.4 GHz. Using different techniques and filters would improve stability, as discussed in this section.

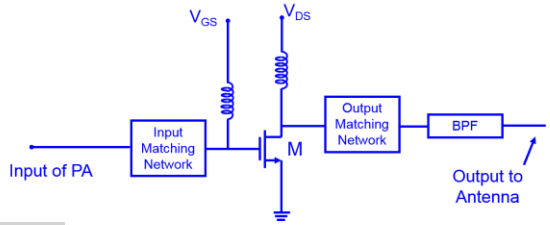


Fig. 1 Schematic Structure of Power Amplifier.

The designing process of a power amplifier typically commences by defining the application, which entails a specific set of figures of merit. Table 1 lists the primary requirements for power amplifier design in Bluetooth systems. The design process of the amplifier was carefully executed to ensure that the requirements were met.

Table 1 Design Goals.

Frequency	2.4 GHz
Bandwidth	>50 MHz
Gain	10 dB
Pin	5 dBm max
PAE Maximum	(>50%)

Figure 2 depicts the proposed amplifier operating at 2.4 GHz. Class AB structure was employed to achieve high performance and ensure high linearity, both of which are key requirements for Bluetooth applications. The FET transistor is used to amplify the input signal at 2.4 GHz with input and output T-matching circuits based on lumped elements. The values of the elements were calculated through a careful design process to minimize reflection at the input and output terminals. The transistor is biased to operate in the chosen class (AB) with a drain-source voltage (Vds) of 3.2 V and gate-source voltage (Vgs) of -1.4 V.

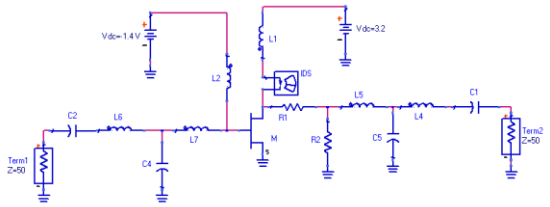


Fig. 2 The Designed Amplifier Circuit Using T-Matching Networks.

The first step of the design was the modeling of I-V characteristics of the transistor at different Vgs values (0 to -2V) and Vds ranging from 0 to 5V, as shown in Fig. 3. To make the transistor operating as a class AB amplifier, the transistor has to be biased in a point that falls between the Q-point of class A and the cut-off region. In the present work, an optimum point, as shown in Fig. 3 (marker-m3), was chosen between the Q-point and cut-off region that has resulted in Vgs and Vds values of -1.4V and 3.2V, respectively, giving an output current of 78 mA, making it a good candidate to deliver high output power with high efficiency.

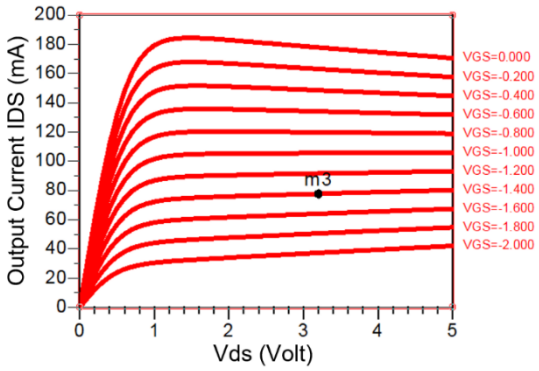


Fig. 3 Characteristics of the Transistor Used in the Present Work.

The stability of the transistor (k) is a crucial factor in improving amplifier performance. This factor mainly depends on the reflection coefficients, as mathematically presented in Eqs. (1) and (2) [18-20].

$$k = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2 * |S_{21}|^2 * |S_{12}|^2} \quad (1)$$

$$\Delta = S_{11} * S_{22} - S_{12} * S_{21} \quad (2)$$

One method to stabilize the transistor is to employ a series and/or parallel resistor at the output side of the transistor to reduce the reflection between the transistor and the load [21, 22]. Increasing the stability of the circuit has been conducted by adding two resistors in series and parallel connection (R1 and R2), as shown in Fig. 4. Tuning and optimization processes were conducted to determine the values of R1 and R2, which were found to be 36 Ohms and 38 Ohms, respectively.

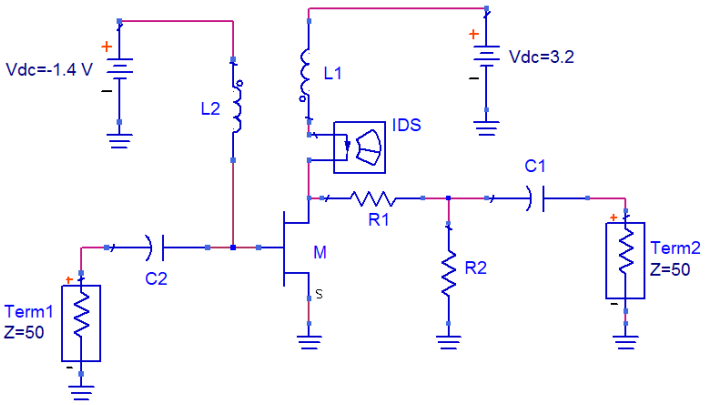


Fig. 4 The Schematic Circuit of the Transistor Using Stability Technique.

The S-parameter of the circuit was simulated, and then the stability was calculated and plotted against the frequency band, as shown in Fig. 5. Figure 5 illustrates the simulated stability with and without the addition of R1 and R2. The value of the stability with R1 and R2 was (k=2.7) compared to a value of 0.35 before adding the resistors. It is clear that the technique used in the proposed approach was highly effective in stabilizing the power amplifier, with a stability factor (k) greater than 1, over a wide range of frequency bands from 1 to 4 GHz.

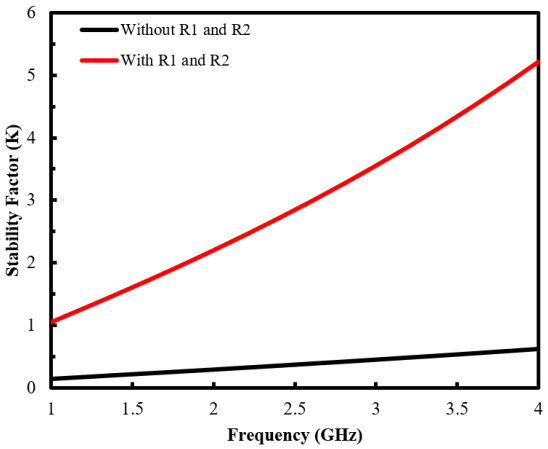
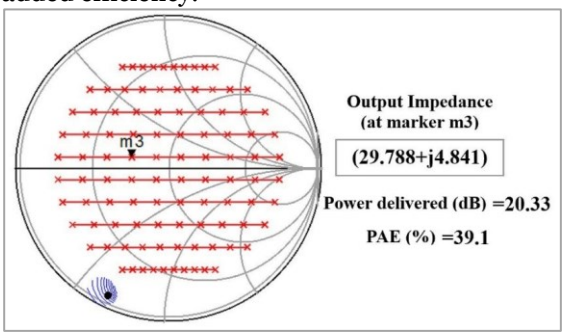


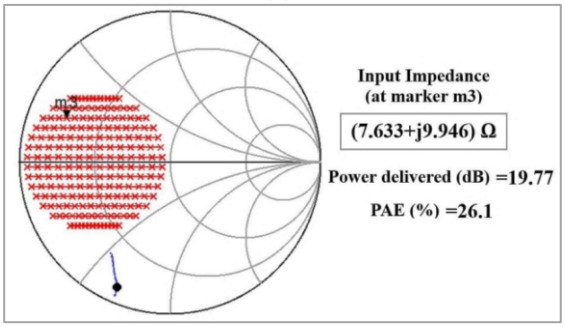
Fig. 5 Stability of the Circuit at 2.4 GHz without Matching Networks.

3.DESIGN PERFORMANCE OF MATCHING NETWORKS

The next stage of designing the amplifier was the design of transistor input and output matching circuits. A matching circuit is crucial for enhancing the total efficiency of the amplifier circuit [23-25]. The design of a matching circuit is challenging and requires a careful process to select the input and output impedances of the transistor at 2.4 GHz. It is well known that the impedance of the transistor varies with the applied DC voltages (Vds and Vgs). The values of Vds and Vgs were fixed at 3.2 V and -1.4 V, respectively, resulting in the source and load impedances of the transistor, as shown in Fig. 6. According to Fig. 6, the extracted transistor's load and source impedances were (29.788 + j4.841) Ω and (7.633 + j9.946) Ω, respectively. These values were selected for the transistor's input and output impedance, as they provide the maximum output power and the highest power-added efficiency.



(a)



(b)

Fig. 6 Simulated Results of (a) Load-Pull (b) Source-Pull of the Transistor.

The design of a matching circuit for two-port devices is a challenging task, as numerous factors must be considered. With proper matching, the transistor will receive and deliver more power, thereby enhancing the performance of the power amplifier. In the present work, careful design steps were taken to design a matching circuit at the input/output sides of the transistor, aiming to minimize the mismatch between the RF source impedance and load impedance, as well as the transistor's impedance. T-matching circuits-based lumped elements were designed and incorporated into this work. Lumped elements have been extensively employed in the design of matching circuits at frequencies up to 5 GHz [26, 27]. The

quality factor (Q) plays a crucial role in determining the matching circuit, bandwidth, and gain of the amplifier. Higher values of the quality factor lead to a narrow bandwidth and high gain in a power amplifier. On the other hand, a small quality factor makes the amplifier unstable. The relation between the Quality factor and bandwidth is given by Eq. (3) [1, 2, 28]:

$$Q = {fo}/{BW} \qquad (3)$$

The designed matching circuits are presented in Fig. 7, showing the values of the elements (inductance and capacitance). Reflection coefficients (S_{11}) of the matching circuits were simulated, and the results are illustrated in Fig. 7. The results clearly indicate a high S_{11} value exceeding -50 dB at the desired frequency. Higher S_{11} values indicate less reflection, resulting in more power being transmitted to the load.

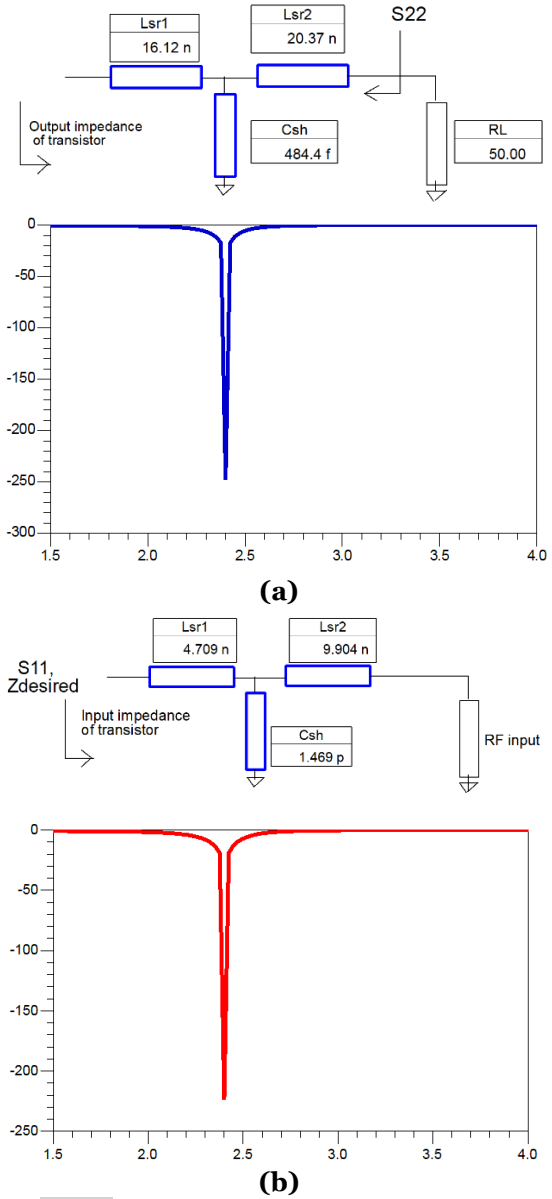


Fig. 7 Schematic Structure of (a) Output Matching and (b) Input Matching Circuits.

4.DESIGN OF BANDPASS FILTER

This work used a BPF filter as an output-matching network to improve power amplifier characteristics. The bandpass filter was utilized in [29] and demonstrated good performance in terms of output power and power-added efficiency (PAE), as discussed in detail in the next section. This section describes the steps involved in designing a resonator bandpass filter. Figure 8 depicts the schematic layout of a tapped Hairpin resonator.

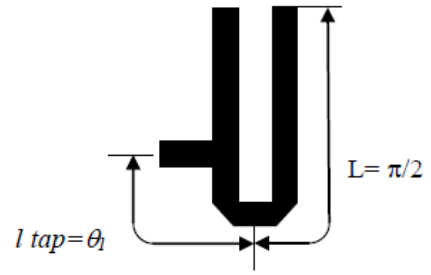


Fig. 8 The Schematic Layout of a Tapped Hairpin Resonator.

The so-called hairpin resonator is a particular kind of U-shaped resonator. To lessen the coupling between resonators, it is vital to reduce the linked line lengths while folding the resonators. In the case of two arms and each hairpin resonator being near each other, they function as a pair of linked lines, which can also impact coupling. Eq. (4) presents the relation between the tapping point (T) and the length of the resonator [30].

$$T = {2L}/{\pi} * \arcsin\left(\frac{\pi}{2} * \left(\frac{Z_o}{Q_e Z_r}\right)\right)^{0.5} \qquad (4)$$

where T is the tap point height, L is the λ/8 of length, Zo is the terminating impedance, Zr is the hairpin line's characteristic impedance, and Qe is the external quality factor. Figure 9 presents the schematic structure of the filter topology of two similar U-shaped resonators. The supply and blockage of the microwave signal are provided by strip conductors on the top side of the circuit. An end connection is used to transport the signal from one resonator to the next. The resonator contour resulted in a filter with a dimension size of 11.7 × 15.3 mm². The performance of the bandpass filter is shown in Fig. 10, represented by the reflection coefficient (S_{11}). It is clear from the simulation result that the passband's lowest transmission coefficient loss (S21) was -0.004 dB. The working frequency range had a fractional bandwidth (FBW) of 4.35% and extends from 2.2 GHz to 2.6 GHz. More importantly, the value of S_{11} was -30.56 dB at 2.4 GHz. It is worth mentioning that the findings of the matching circuit and filter were excellent, demonstrating the effectiveness of the techniques used in the present work, which would clearly improve the performance of the amplifier circuit.

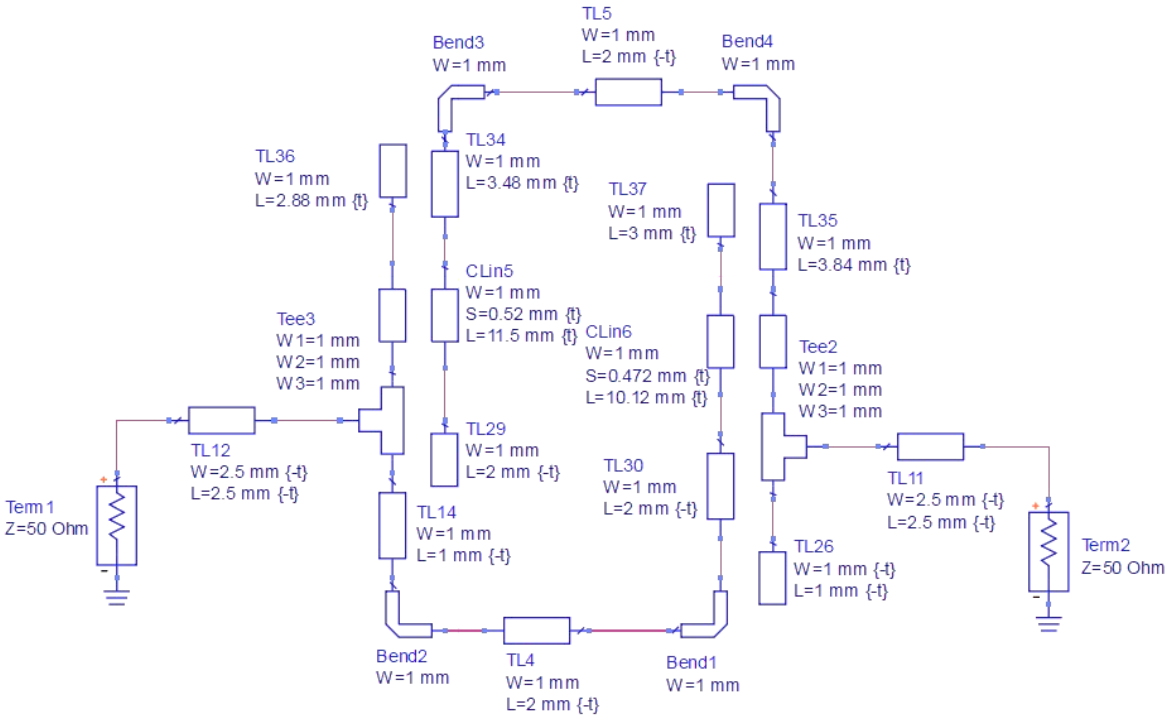


Fig. 9 Schematic Design of the Bandpass Filter Used in the Present Work.

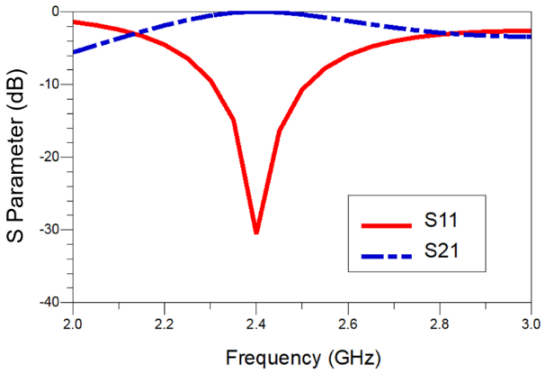


Fig. 10 Simulated S-Parameter of the Filter.

5.POWER AMPLIFIER PERFORMANCES

The integrated power amplifier with the bandpass filter is depicted in Fig. 11, which includes R1 and R2 as stabilizing elements. To reduce the circuit size and improve power handling, the output matching circuit was replaced with a custom-designed bandpass filter placed between the transistor and the output load. This step also reduces the number of transmission lines used and losses, which is highly beneficial in the fabrication of low-cost, low-power, and small-size power amplifier circuits.

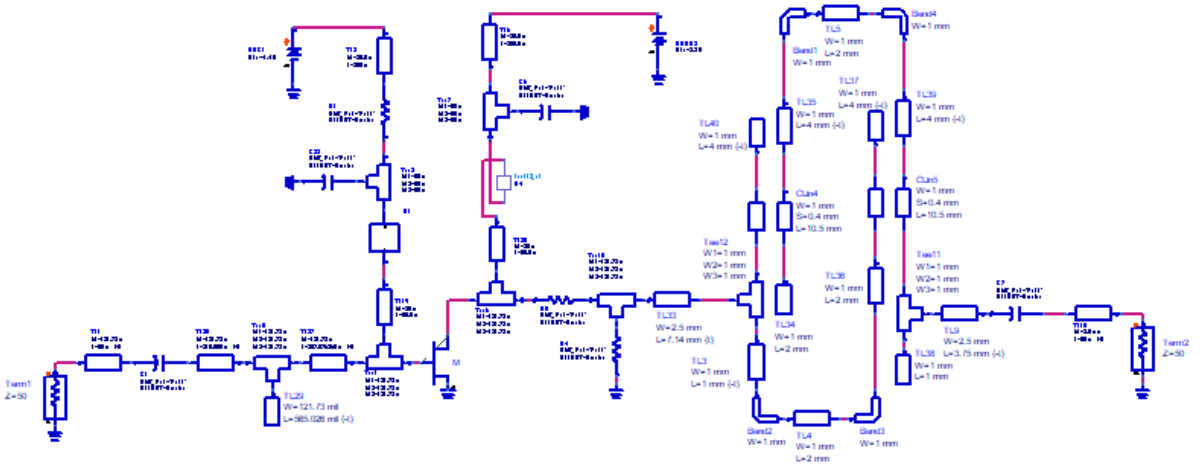


Fig. 11 The Schematic Design of Power Amplifier with Bandpass Filter.

To validate and verify the design, the schematic design of the circuit was then transformed into the Momentum platform of ADS to create the layout designs, as shown in Fig. 12. A FR4 substrate with a permittivity of 4.3 and a loss tangent of 0.025 was employed. A copper with a thickness of 0.035 mm was used to make the transmission lines. The length of transmission lines was calculated using the line calculation tool in the ADS software. The optimum size of the circuit was 57 × 32 mm², as depicted in Fig. 12.

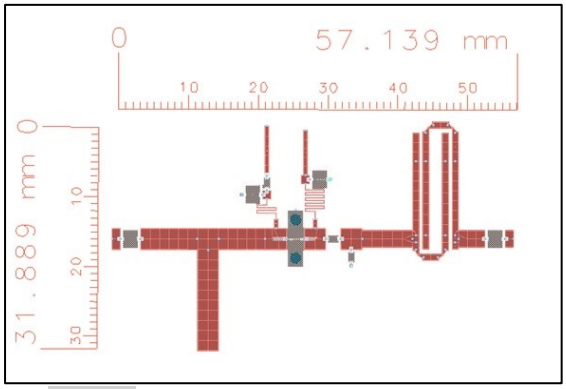


Fig. 12 Layout of the Amplifier Circuit.

Momentum simulation was used to simulate the S-parameter of the amplifier over the frequency band from 1.0 GHz to 3 GHz, as shown in Fig. 13. The results included the simulated values of S_{11} of the schematic (straight line) and layout (dotted line) designs in brown color, where a bandwidth of 100 MHz can be achieved from the proposed amplifier. Higher values of S_{11} and S_{22} were obtained for both designs, with values of ~-24dB and ~-20dB, respectively, at 2.4 GHz. These values are comparable to those reported in [13, 14] and better than the reflection in [15], where very low reflections of S11 and S22 were obtained between 0 and -10 dB in the frequency band of room 1 to 3 GHz. The simulated gain represented by S_{21} exceeded 10 dB at the desired frequency (2.4GHz), which proves that the proposed design is highly compatible with other works, where simulated gains ranging from 10 to 16 dB were achieved using class AB power amplifier-based GaN and GaAs FET devices [15, 31], as well as class F power amplifier based GaN HEMT device [32]. Moreover, the gain of the proposed amplifier meets the requirements of Bluetooth applications. The simulated S_{12} value, which exceeds -25 dB for both layout and schematic designs, is comparable to those reported in [12-15]. This result proves that the matching networks and BPF used in this work were sufficiently efficient in blocking the signal from the output to the input side, thereby reducing the leakage current that could deteriorate amplifier performance.

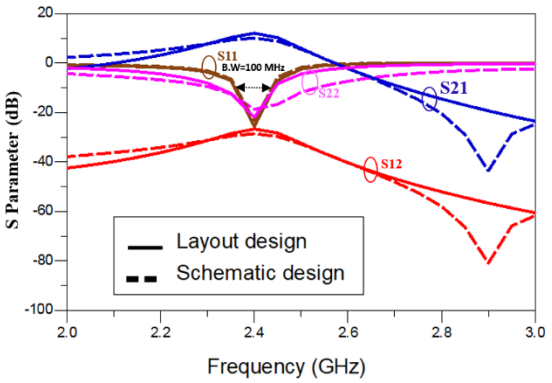


Fig. 13 S-Parameter Result of the Amplifier Circuit.

The maximum available gain (MAG) of the amplifier was simulated against frequency, as shown in Fig. 14, and found to be 12.7 at 2.4 GHz. The MAG can be calculated using the S-parameter and reflection coefficients, as expressed in Eq. (5) [1, 2], where Γ_S and Γ_{Out} represent the source and load reflection coefficients.

$$MAG = \frac{1-|\Gamma_S|^2}{|1-S_{22}\Gamma_S|^2}\,|S_{21}|^2\,\frac{1}{1-|\Gamma_{Out}|^2} \qquad (5)$$

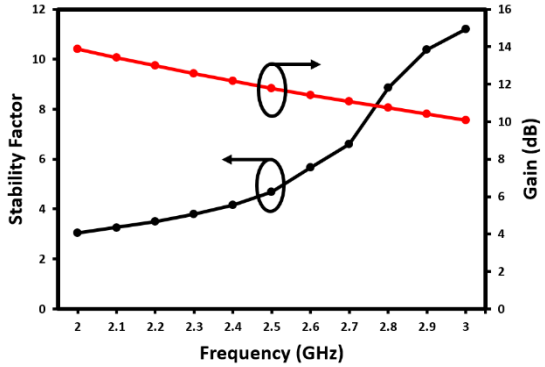


Fig. 14 Simulated Gain (red line) and Stability (Black Line) of the Amplifier Circuit.

Figure 14 also includes the value of the stability factor (k) for the final design, which is 4.27 at 2.4 GHz, significantly higher than the values obtained from the simulation results in Refs. [14, 15]. This result implies that the proposed design is highly stable at the desired band, which is certainly due to the use of stabilizing resistors, matching networks, and a bandpass filter at the amplifier's output. Figure 15 depicts the output power spectrum of the amplifier at 0 dBm input RF power, indicating that the output power was 15.95 dB at the fundamental frequency (2.4 GHz). The matching circuit and filter have been optimized to suppress the second and third harmonics, resulting in a power level of less than -20 dBm for the 2nd and 3rd harmonic components. Giving a separation of nearly 35 dBm between the fundamental and second harmonic. This figure is very close to the harmonic level of -20 dBm attained in [15], with a separation of approximately 40 dBm. It is critical to reduce the harmonics power level and ensure that no performance deterioration occurs in the following stages of the system.

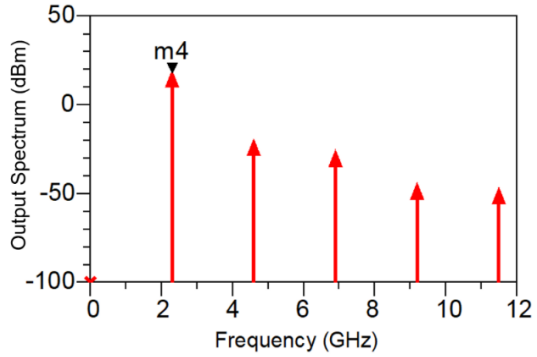


Fig. 15 Output Spectrum of the Proposed Power Amplifier at 0 dBm Input RF Power.

The output power was simulated as a function of the input RF power from -10 dBm to 20 dB, as depicted in Fig. 16. At -10 dBm and 5 dBm input RF power, the proposed amplifier can deliver an output power of 5 dBm and 20 dBm, respectively, which agrees well with the power requirements of Bluetooth connection of class 2 (up to 10 m) and class 1 (up to 100 m) [33]. The amplifier's output power saturated at ~7 dBm of input RF power, reaching a maximum value of ~22 dBm. Making the amplifier a suitable candidate for various applications, such as Long-Term Evolution (LTE) [34]. For comparison with other reported works, the output power of the proposed amplifier aligns well with the performance of the GaAs FET amplifier in [14], where a simulated output power of 16 dBm was achieved at an input RF power of 5 dBm. In Refs. [29, 32], higher simulated output power of ~40 dBm was reported for the GaN HEMT amplifiers at high input RF power and high drain voltage of 30 dBm and 28 V, respectively, inevitably leading to high power dissipation, which is a key factor in determining the performances of low power applications.

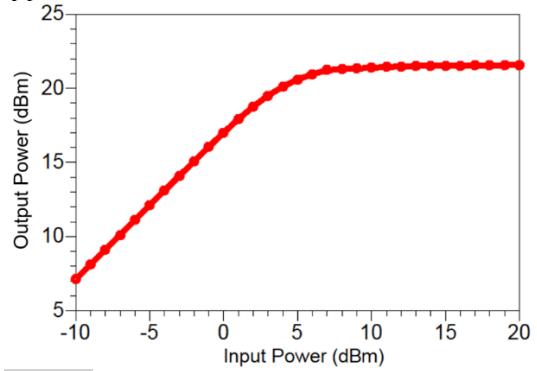


Fig. 16 Output Power Versus Input RF Power at 2.4 GHz.

The result in Fig. 17 (a) presents the relationship between the output power and the amplifier gain (1 dB compression), showing that the gain decreases by 1 dB when the output power reaches 17 dBm. The result in Fig. 17 (b) shows that the amplifier maintained a constant gain over a wide range of input RF power, from ~4 dBm to 12 dBm. Moreover, the maximum power-added efficiency was 67.8% at ~8 dBm input RF power, which is highly comparable to the values reported in [29, 32], where a similar approach using transmission line matching networks and a bandpass filter (BPF) at the output side of the amplifier was employed.

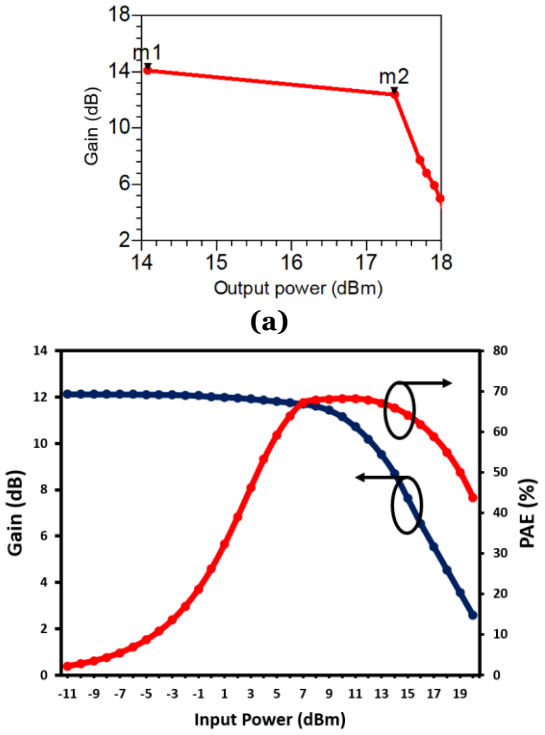


Fig. 17 Simulation Results (a) Power Gain Versus Output Power, (b) PAE and Power Gain Versus Input Power in dBm.

Table 2 compares the performances of the proposed amplifier with other reported simulation and experimental works [12- 15, 29, 31, 32, 35], including output power, gain, PAE, B.W, stability factor, and S-parameters. It can be said that the present design has achieved an acceptable figure of merit with a relatively small circuit size compared to other reported works, which makes it a promising design for implementation in Bluetooth and LTE systems. It is ample that the present amplifier performances can compete with the simulated performances of class AB GaAs amplifiers reported in [12-14] in terms of output power, S11, S12, S21, and S22 data. Furthermore, the proposed design recorded a better stability factor and PAE values compared to amplifiers in [12-14], where very low stability factor and PAE were achieved in [14] with a value of 0.9 and 11.2 %, respectively, compared to 4.27 and 68.7 % obtained in this work. This result is certainly due to the design process, which considered several factors that impact overall performance, as well as the optimized designs of matching networks and filters, which play a crucial role in determining the output power and power-added efficiency (PAE) of the amplifier. However, the proposed amplifier

exhibited a narrow bandwidth of 100 MHz, compared to 1700 MHz and 1800 MHz in [14, 15], which is a direct result of using a Microstrip transmission line in the design of the matching networks and BPF circuit. Table 2 also lists the performances of power amplifiers based GaN transistors [29, 31, 32, 35], where it is clear that these devices provide a considerably high output power and PAE, however, at the expense of high drain voltages (28 V) and high input RF power (>20 dBm). Making these amplifiers consume high DC power could limit their uses in applications where power dissipation is a critical factor. On the other hand, the proposed PA achieved an acceptable output power of 22 dBm at a low input RF power of 7 dBm and a low drain-to-source voltage of 3.2 V. Clearly, the proposed PA consumes less power compared to the aforementioned previously reported PAs, which makes it more compatible with the modern wireless communication circuits. The total size of the proposed circuit is comparable to the size of the circuit reported in Ref. [29] (57 × 32 mm² for our design and 57 × 42 mm² for [29]). While it is smaller in size compared to the amplifier circuits reported in Ref. [12, 13]. Reducing the size of the circuit enables the integration of more circuits into a single chip. Thus, higher output power can be achieved. Finally, the output power, gain, and PAE comparisons showed that the proposed PA circuit had nearly superior performance, as demonstrated in Table 2. Additionally, the proposed PA's size was 10–20% smaller than that of the PAs in previous studies. In terms of comparing the functionality of BPF, the suggested method provides the simplest way to construct the OMN. Owning to the fact that the proposed BPF firstly selects the frequency and suppresses the harmonics, and secondly, it acts as a matching network that delivers maximum power to the output terminal.

Table 2 Compares the Performances of the Proposed Amplifier with other Reported Simulations and Experimental Works.

Ref	[12]	[13]	[14]	[15]	[29]	[31]	[32]	[35]	This work
Frequency (GHz)	2.45	2.6	1.5-3	1.2-3	2.1- 2.8	1-3	1.2-3.6	1.45-2.55 (Center @2 GHz)	2.4
Filter type	Microstrip LPF	Microstrip BPF	None	BPF	Microstrip BPF	Novel BPF	Coupled line LPF	elliptic LPF	Microstrip BPF
MN type	T section	L section	None	L section	None	T-type and π -type	None	L section	T section
Transistor	GaAs-FET	LD-MOSFET	GaAs FET	GaAs FET	GaN HEMT	GaN FET	GaN HEMT	GaN HEMT	GaAsFET
Class of operation	Class-AB	Class-AB	None	Class AB	Class F	Class AB	Class F	None	Class-AB
Output power (dBm)	14 @ 7 dBm input RF power	25 @ 10 dBm input RF power	16 @5 dBm input RF power	46 @ 35 dBm input RF power	40 @ 24 dBm input RF power	40	40	42.5	22 @ 7 dBm input RF power
B.W (MHz)	100	100	1700	1800	700	2000	2400	1100	100
PAE (%)	-	46.3	11.2	None	75	53	70	70–84	68.7
S11 (dB)	-38	-22	-10 to -21	0 to -7	None	Below -12	None	-40	-32
S12 (dB)	-23	-21	-20 to -25	-60 to -30	None	none	None	-	-33
S21 (dB)	19.4	14.4	10-16.7	-17 to 10	18 @ 2.4GHz	14- 15.5	11	10.8–14.8	12.7
S22 (dB)	-33.5	-8	-15 to -22	0 to -10	-35 @ 2.4GHz	none	None	-	-23
Stability factor (k)	1.158	-	0.8-0.9	1- 1.3	None	none	None	-	4.27
Total size (mm²)	73.5 × 36	90 ×70	None	None	57 × 42	none	42 ×34	-	57 × 32

6.CONCLUSIONS

In the present work, a high-performance integrated single-stage power amplifier with a bandpass filter was designed and simulated using the ADS tool. GaAs FET MGF2407A transistor was used as the primary active device to amplify the signal at 2.4 GHz. The large-signal simulation demonstrated that the proposed power amplifier, PA-BPF, achieved a maximum output power and power added efficiency (PAE) of 22 dBm and 68.7%, respectively, at a 7 dBm input RF power level. Furthermore, the proposed design provided a power gain of 12.7 dB at 2.4 GHz, and more importantly, the amplifier unconditionally stabled with a stability factor higher than 3 over the band (2 to 3 GHz). Using the BPF neglected the need to employ a matching circuit, which significantly contributed to the circuit's good output power and small size. To summarize, the

amplifier-based GaAs transistor is a promising candidate for 2.4 GHz applications, offering high output power and gain, high power-added efficiency, and a compact area size. With further optimization of the matching circuit and bandpass filter, as well as the use of transistors with high drain current, amplifier performance can be improved for a range of applications. Moreover, the design process employed in this work can play an increasingly significant role in designing mm-wave and sub-mm-wave power amplifiers.

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NOMENCLATURE

A	Area, mm^2
BW	Bandwidth
f_o	Operational frequency, Hz
I	Current, A
I_{DS}	Drain-Source current, A
k	Stability factor
L	λ/8 of length, m
Q	Quality factor
Qe	External quality factor
R	Resistance, Ω
V_{DS}	Drain-Source voltage, V
V_{GS}	Gate-Source voltage, V
T	Tap point height, m
Zo	Normalize impedance, Ω
Greek symbols	
Ω	Unit of resistance measurement
Γ_S	Source reflection coefficients
Γ_{Out}	Load reflection coefficients
λ	*Wave* length, m

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