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Design and Implementation of a Cpld-Based Multilevel Inverter Depending on a Complex Programmable Logic Device (CPLD)

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Abstract

A complex programmable logic device (CPLD) based multilevel inverter has been designed and implemented. The design involves three main parts. The first part is the switching angle generator (SAG), which determines the switching angles from an optimized primitive angle. The second part is the switching pulse generator (SPG), which controls the drive circuit of the inverter. The timing circuit is the third part, which provides the necessary timing for both SAG and SPG. Implementing both SAG and SPG using a CPLD device mean high speed cycle time. Hence an accurate timing for the switching angles is obtained compared to other procedures that uses software for calculating and generating the switching angles, such as microcontroller. MATLAB work space has been used to acquire and analyze the inverter output via the PC sound card. Results of the implemented inverter staircase output voltage, as well as the output frequency spectrum are obtained.

Keywords: Multileve Inverter, Switching-Angles, Optimized Harmonics, CPLD

تصميم وتنفيذ عاكس متعدد المستويات بالاعتماد على الدوائر المنطقية المبرمجة المعقدة (CPLD)

الخلاصة

تم تصميم وتنفيذ عاكس متعدد المستويات بالاعتماد على الدوائر المنطقية المبرمجة المعقدة (CPLD). يتضمن التصميم ثلاث أجزاء رئيسية، ألجزء الأول هو مولد زاوية القدح الذي يحدد زوايا القدح باشتقاقها من الزوايا الأولية المحسوبة مسبقا للحصول على أفضل أداء بينما كان ألجزء الثاني مولد نبضات القدح التي تسيطر على دائرة السوق للعاكس في حين تمثل دائرة التوقيت الجزء الثالث والتي تجهز التوقيتات الضرورية لدائرتي الجزء الأول والثاني. إن تنفيذ مولد زوايا القدح مع مولد نبضات القدح باستخدام الدوائر المنطقية المبرمجة المعقدة يعطي سرعة عالية لزمن دورة التنفيذ cycle time مما يؤمن دقة عالية لزوايا القدح بالمقارنة مع التقنيات الأخرى التي تستخدم البرمجيات لحساب وتوليد زوايا القدح مثل المسيطر الدقيق micro-controller. تم استخدام برنامج (MATLAB) لكسب وتحليل فولتية إخراج العاكس من خلال بطاقة الصوت للحاسوب الشخصي. تم الحصول على فولتية الإخراج بشكلها السلمي بالإضافة إلى طيفها الترددي.

الكلمات الدالة: العاكس المتعدد المستويات، زوايا القدح، الدوائر المنطقية المبرمجة المعقدة.

Introduction

Cascaded H-Bridge Inverter

The multilevel inverters have a unique structure [1-2] allowing them to reach high voltages with low harmonics. The general function of multilevel inverter is to synthesize a desired voltage from several levels of dc voltages. The popular type structure of the multilevel inverter is the cascaded H-Bridge type. This type of inverter consists of full bridge or H-bridge inverters connected in series, and the output voltage is equal to the sum of the outputs of all H–bridge

inverters. Fig. (1) Shows a single phase configuration where V_{AN} represents the output phase voltage. The output of each H-bridge can be controlled by four switches. The output phase voltage levels are defined by m=2k+1, where k is number of levels and is the number of DC sources.

Optimized Harmonics Stepped Waveform

Using Fourier series expansion of the (stepped) output voltage waveform of the multilevel inverter shown in Fig. (2), the output voltage $V(\omega t)$ can be written as follows [3- 5]:

$$V(\omega t) = \frac{4V_{DC}}{n\pi} \sum_{n=1,3,5,\ldots}^{\infty} \begin{pmatrix} \cos n\alpha_1 + \cos n\alpha_2 + \\ \ldots\ldots\ldots + \cos n\alpha_n \end{pmatrix} * \sin n\omega t \ldots\ldots\ldots\ldots\ldots\ldots (1)$$

Where V_{DC} is the DC level voltage

n is an odd harmonic order

The normalized magnitude of Fourier coefficients $H(n)$ with respect to V_{DC} can be written as:

$$H(n) = \frac{4V_{DC}}{n\pi} \sum_{L=1}^{K} \cos(n\alpha_L) \ldots\ldots\ldots\ldots\ldots\ldots (2)$$

According to Fig. (2), the angles $\alpha_1 to\ \alpha_k$ must satisfy the following condition $\alpha_1 < \alpha_2 < \ldots < \pi/2$. The goal is to eliminate the lower dominated harmonics, and filter the higher residual frequency. From Equation (2), the amplitude of odd harmonic components in a quarter-wave symmetry of a multilevel waveform is:

$$H(n) = \frac{4V_{dc}}{n\pi} \left[\cos n\alpha_1 + \cos n\alpha_2 + \cos n\alpha_k\right] \ldots (3)$$

where n = 1, 3, 5, 7,

The set of non-linear equations corresponding to Eq.(3) can be given as follows:

$$\frac{4V_{Dc}}{\pi} \begin{bmatrix} \cos(\alpha_1) + \cos(\alpha_2) + .. + \\ \cos(\alpha_{k)} \end{bmatrix} = H_1 \ldots (4)$$

$$\frac{4V_{Dc}}{3\pi} \begin{bmatrix} \cos(3\alpha_1) + \cos(3\alpha_2) + .. + \\ \cos(3\alpha_{k)} \end{bmatrix} = H_3 .. (5)$$

$$\frac{4V_{Dc}}{5\pi} \begin{bmatrix} \cos(5\alpha_1) + \cos(5\alpha_2) + . + \\ \cos(5\alpha_{k)} \end{bmatrix} = H_5 .. (6)$$

$$\frac{4V_{Dc}}{n\pi} \begin{bmatrix} \cos(n\alpha_1) + \cos(n\alpha_2) + . + \\ \cos(n\alpha_{k)} \end{bmatrix} = H_n .. (7)$$

where H_1 is the amplitude of fundamental component at (n = 1), and H_n is the amplitude of the n^{th} component. The set of nonlinear Equations (4-7) can be solved by iterative methods such as Newton-Raphson method or by using trigonometric identities to expand the terms $\cos(n\alpha_n)$ and then using resultant theory [6]. The switching angles may also be solved to minimize total harmonic distortion. The THD for the voltage waveform may be written as [7].

$$THD(\%) = \frac{\sqrt{\sum_{n=2}^{\infty} (H(n))^2}}{H_1} \ldots\ldots\ldots\ldots\ldots\ldots (8)$$

The modulation index M of the specified multilevel inverter is defined as follows [3]

$$M = \frac{V_L^{\ *}}{V_{L\max}} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (9)$$

Where $V_L^{\ *}$ is the amplitude command of the inverter output voltage (H_1). $V_{L\max}$ is the maximum attainable amplitude of the inverter. Five level inverter (m = 5) = 2k +1 is constructed with two DC source (k = 2), therefore two H-bridges with two switching angle equations can be written to eliminate the harmonic component.

$$\cos(\alpha_1) + \cos(\alpha_2) = \frac{kM\pi}{4} \ldots\ldots\ldots\ldots\ldots\ldots (10)$$

$$\cos(3\alpha_1) + \cos(3\alpha_2) = 0 \ldots\ldots\ldots\ldots\ldots\ldots (11)$$

Solving above equations using Newton-Raphson method, values of α_1, α_2 and THD are obtained for different values of modulation index M and are given in Table (1). In the waveform shown in Fig. (2), the first quarter cycle has a zero output voltage level from $\omega t = 0$ to $\omega t = \alpha_1$. At $\omega t = \alpha_1$, the output voltage level is changed from zero to $+V_1$, and from $+V_1$ to $+ (V_1+V_2)$ at $\omega t = \alpha_2$. The process will be repeated until $\omega t = \pi/2$, and the output voltage level becomes $+V_1$, $+V_2$, … $+V_{(k-1)}$, $+V_k$. Then in the second quarter, the level of the output voltage will be decreased to $+V_1, +V_2, +\ldots V_{(k-1)}$ at $\omega t = \pi - \alpha_k$. The process will be repeated until $\omega t = \pi-\alpha_1$ and output voltage becomes zero again. In the second half cycle of the waveform, the process will be repeated as in the previous steps except the changes in the dc sources amplitudes from positive to negative. The next period will then be repeated in the same sequence as in the first cycle. In this work, the first set of angles (α_1, α_2), which corresponds to the minimum THD in (Table1), are chosen. To obtain a symmetrical output waveform, eight switching angles can be derived from the primitive switching angles (α_1, α_2) as shown in (Table 2).

Inverter Implementation

The inverter can be implemented in three methods. The first is the old traditional methods that uses either fixed function integrated circuits or microcontrollers **[8].** The first method suffer from flexibility lack, while the second has limited performance due to low level programming. Recent advances in PLD devices has drawn much attention due to their shorter design cycle, high computation speed that can ensure the accuracy of the instants that gating signals **[9]**. In this work, CPLD (ATF1508AS of Atmel) is used to implement the inverter.

CPLD Implementation of Control Circuit

CPLD had made a revolution in implementing control circuits in the field of gating drives for inverters **[10].** Fig. (3) Shows a block diagram of the inverter system. The control circuit is implemented on a Complex Programmable Logic Device (CPLD). The CPLD is driven by a clock CLK of 1 MHz, and a reset CLR signal to initialize the circuit. The CPLD is fed with the primitive optimized angles (α_1 and α_2 , which are calculated off-line, and then the CPLD calculates the switching angles which are derived from the primitive angles, and generates the appropriate switching pulses. These switching pulses are fed to the 5- level inverter. The control circuit has been designed using the CAD software MAX+PLUS II (ver. 10.0) of Altera**[11].** The schematic capture approach is chosen to implement the design (Fig.4). The main function of the control circuit is to generate eight gate pulses for eight MOSFETs which act as switches (S_{11}, S_{12}, S_{13}, S_{14}, S_{21}, S_{22}, S_{23}, and S_{24}) for a 5-level inerter (Fig.1). The control circuit can be divided into three main sections; the timing circuit, the switching angles generator (SAG), and the switching pulses generator (SPG). The timing circuit includes two binary counters. The first is a 16-bit up counter, which is driven by an external 1 MHz clock (CLK) to provide an accuracy of 1 µS in determining the time positions of the switching angles. Since a 50 Hz sine wave has a time period of 20 mS, the switching angle could be any number between (0-20000 µS). Hence the 16-bit counter should count from (0 to 20000) repeatedly. The second counter is a 4-bit binary counter. This counter is driven by a clock from the output (A=B) of a 16-bit comparator. This counter provides the timing for the eight switching angles.

Notice that only the least three significant bits are used from the outputs of this counter, since only 8-states are required corresponding to 8 switching angles. The comparator compares between the output of the 16-bit counter and the next angle which is calculated by SAG circuit, and it produces a pulse when the counter output reaches the switching angle. Hence the comparator produces 8 pulses during one cycle of a 50 Hz sine wave. These pulses drive the clock of the 4-bit counter. An external clear (CLR) signal is provided for the timing circuit to initiate all flip-flops, and counters. The SAG circuit includes four multiplexers and an adder ⁄subtracter. Both are controlled by the outputs of the 4-bit counter. The main function of the SAG circuit is to calculate the next angle in time domain from the optimized primitive angles (in case of 5-level inverter, two angles α_1, and α_2 according to Table 2). The four multiplexers select two parameters to be either added or subtracted by the adder ⁄subtracter. Therefore, the eight angles are calculated sequentially and sent to the comparator input in the timing circuit. The SPG circuit consists of a 2 to 4 decoder, four j-k flip-flops, and four d-type flip-flops. Since in each switching mode there is a switch which is switched ON, while another is switched OFF (Table 3), the control signals of the eight switches (of a 5- level inverter) can be reduced to only four signals. The other four signals can be derived by complementing the first four signals. The four j-k flip-flops outputs provide the first four signals, while the four d-type flip-flops provide the other four signals after complementing the first four signals. The presence of the d-type flip-flops which are triggered by the positive edge of the main CLK is to provide a delay of less than 1μS to prevent a short circuit on the supply batteries during switching. Revising (Table 3), enable to conclude that there is only four switching sequences in the first half of the cycle. The same switching sequence is being repeated in the next half cycle. Hence a 2 to 4 decoder whose inputs are taken from least two significant bits (D0, D1) of the 4-bit counter, can be used to clock the j-k flips-flops (Fig. 4). Having built the control circuit in MAX+PLlUS II software, the circuit is simulated and the simulation results are shown in Figure(5). Then the circuit data file is downloaded into the CPLD to get the actual pulses which drive the MOSFETs main power switches.

Results

Simulated Results

Simulated results for m=1, the switching angles $\alpha_1=5.08^\circ$ and $\alpha_2=54.9^\circ$ (from Table 1), shows that the THD has minimum value and an RMS output voltage = 220V (for equal H bridge input when DC voltage = 120V) as shown in Figure (6), compared with m=0.8, switching angles $\alpha_1=13.48^\circ$ and $\alpha_2=73.48^\circ$ an RMS output voltage = 170V as shown in Figure (7).

Practical Results

Figure (8) shows the obtained output voltage waveform for the implemented 5-level inverter for m=1 . The frequency spectrum for the 50Hz output is shown in Figure (9). The fundamental component has the highest magnitude, while the harmonic components have a decreasing magnitudes. The CPLD input parameters are set to give an output frequency of 50Hz. Any other desired frequency can be attained by simply adjusting the input frequency of the CPLD without any changes in the schematics of the inverter.

Conclusions and Suggestions

1. Implementing both (SAG) and (SPG) using CPLD meant high flexibility to change both (α_1 and α_2) and the input clock frequency. Hence the inverter output RMS voltage and its frequency can be changed easily.
2. Inverter applications such as speed control of AC motors can be easily carried out using the proposed inverter. This is of a great benefit compared with other implementations of the inverter based on micro-controllers or fixed function integrated circuits.

It is suggested to introduce the calculation of the primitive angles to be held in system by adding a unit of digital signal processor (DSP) before the CPLD unit , thereby getting a fully automotive inverter.

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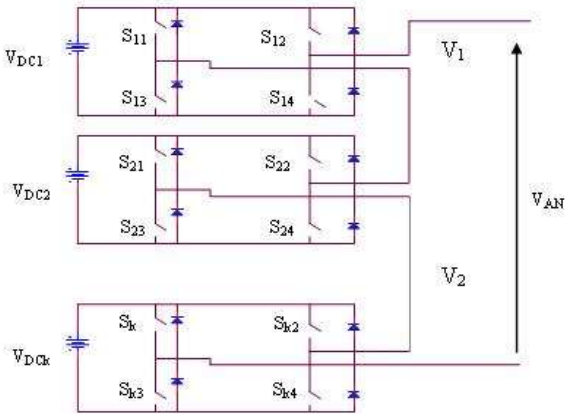


Figure (1) single phase configuration for m-level inverter in cascaded form

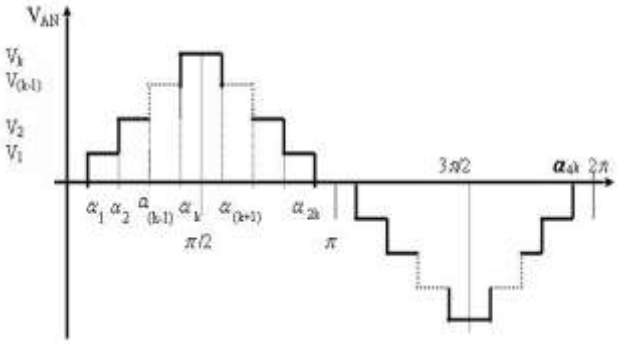


Figure (2) Output voltage waveform of m-level inverter

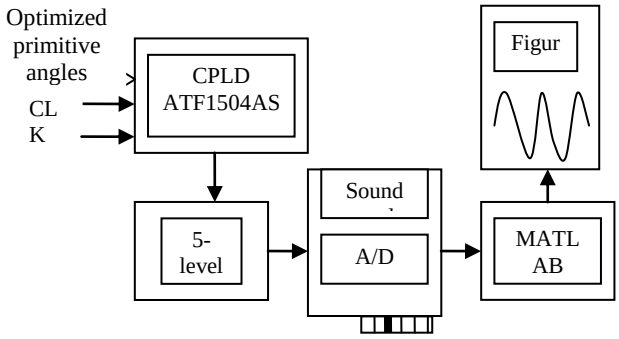


Figure (3) Block diagram of the proposed inverter system

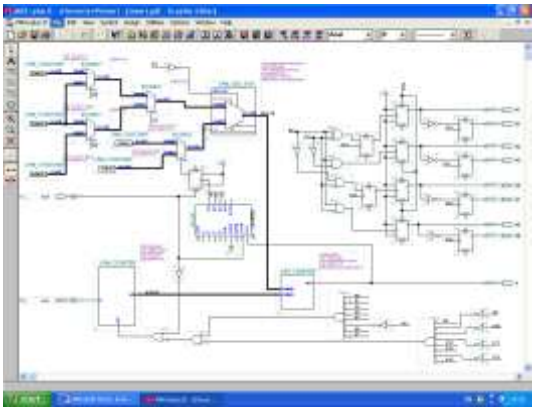
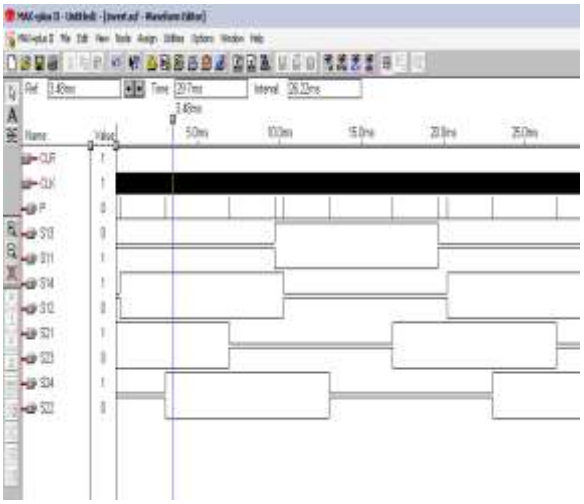


Figure (4) CPLD schematic of the implemented inverter using MAX+PLUS II



Figure(5) Simulated gate pulses using MAX+PLUS II software

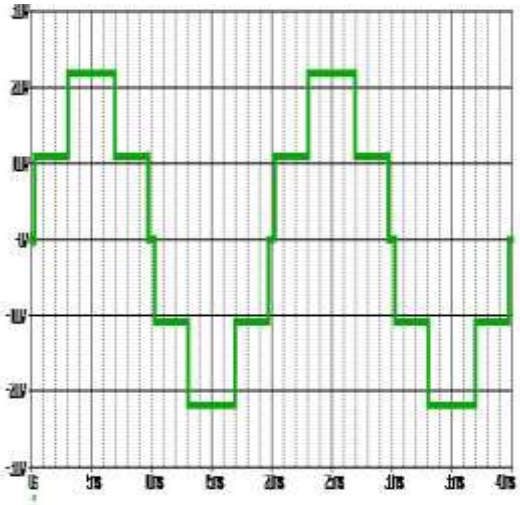


Figure (6) Simulated inverter output for m=1 , α_1=5.08° and α_2=54.9

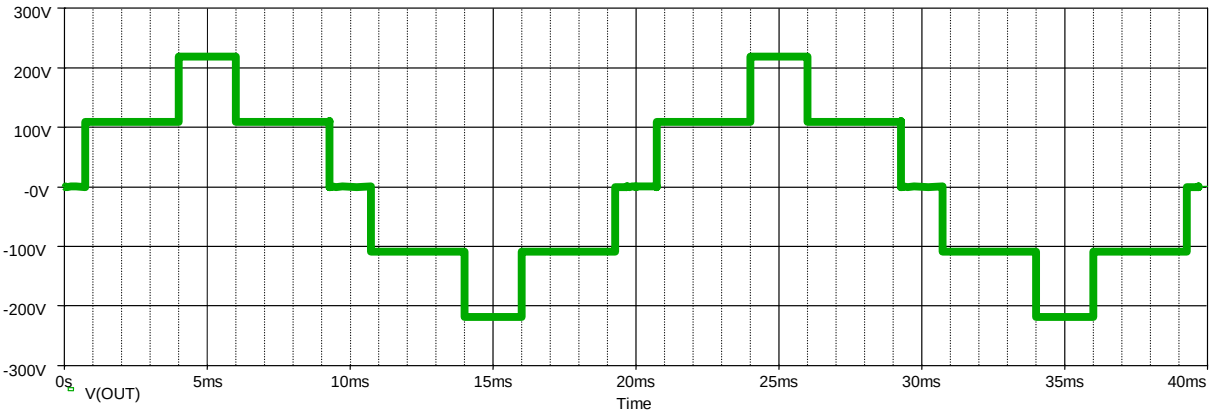


Figure (7) Simulated inverter output for m=0.8, α_1=13.48° and α_2=73.48°

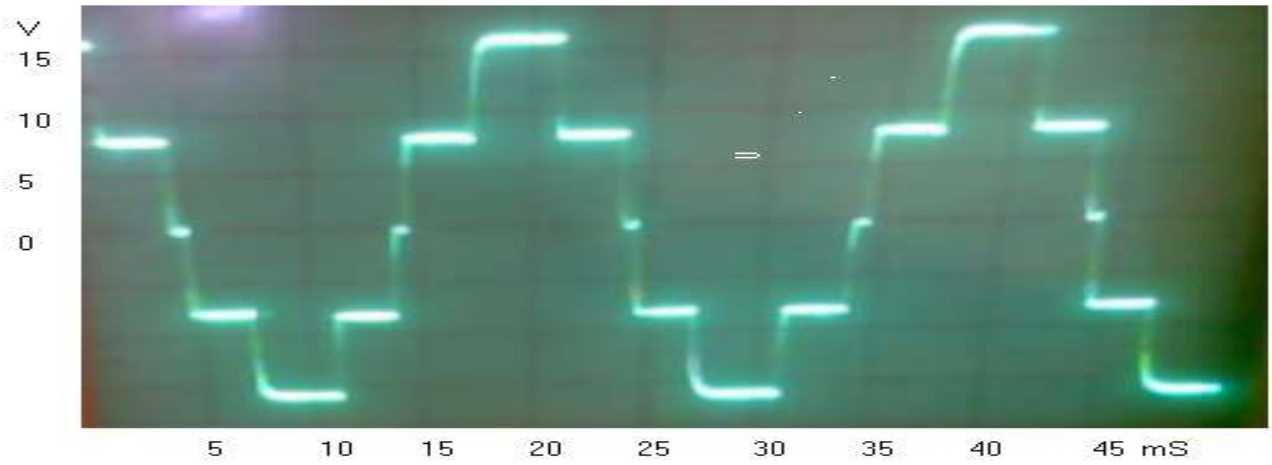


Figure (8) Practical inverter output waveform m=1 , α_1=5.08° and α_2=54.9

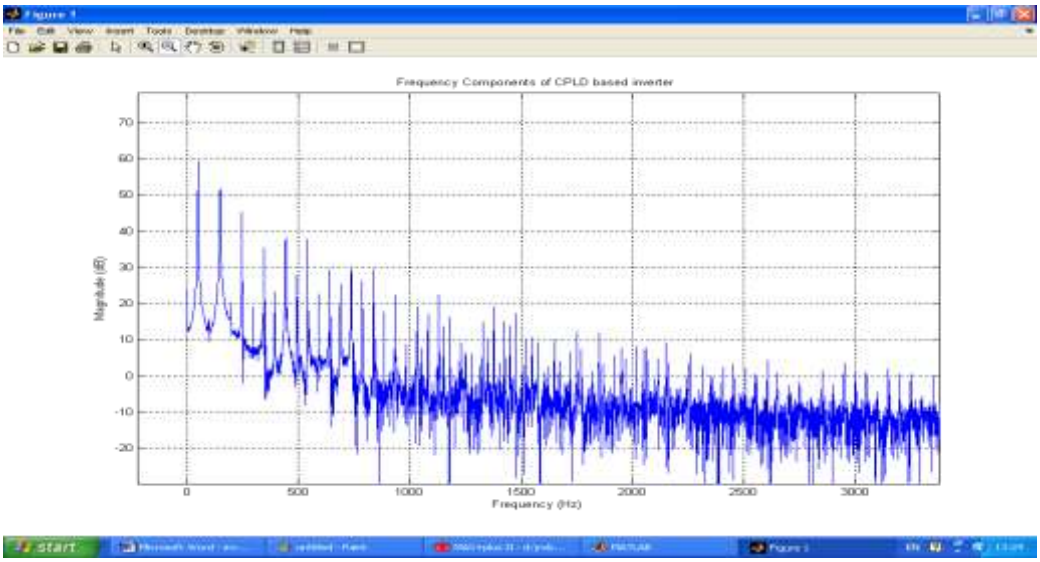


Figure (9) Frequency spectrum of the inverter output

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Table (1) The output voltage THD corresponding to the switching angles for 5-level inverter

Modulation Index M	α_1, (Degree)	α_2, (Degree)	THD, (%)
1.0	5.08	54.91	25.16
0.95	0.50	60.50	30.66
0.9	5.29	65.29	29.54
0.85	9.56	69.29	29.58
0.8	13.48	73.48	30.27
0.75	17.14	77.14	31.25
0.7	20.59	80.59	32.19
0.65	23.87	83.87	32.70
0.6	27.03	87.03	32.37

Table (2) The switching angles and the equivalent time periods

	The angle in degrees	Equivalent time period in µS
1	$\alpha_1 = 5.08$	282
2	$\alpha_2 = 54.91$	3051
3	$\pi - \alpha_2 = 125.09$	6949
4	$\pi - \alpha_1 = 174.92$	9718
5	$\pi + \alpha_1 = 185.08$	10282
6	$\pi + \alpha_2 = 234.91$	13051
7	$2\pi - \alpha_2 = 305.09$	16949
8	$2\pi - \alpha_1 = 354.92$	19718

Table (3) Power switches states for 5-level inverter

Switching angle interval	S_{11}	S_{12}	S_{13}	S_{14}	S_{21}	S_{22}	S_{23}	S_{24}	Vout
0 to α_1	1	1	0	0	1	1	0	0	0
α_1 to α_2	1	0	0	1	1	1	0	0	+Vdc
α_2 to $(\pi - \alpha_2)$	1	0	0	1	1	0	0	1	+2Vdc
$(\pi - \alpha_2)$ to $(\pi - \alpha_1)$	1	0	0	1	0	0	1	1	+Vdc
$(\pi - \alpha_1)$ to $(\pi + \alpha_1)$	0	0	1	1	0	0	1	1	0
$(\pi + \alpha_1)$ to $(\pi + \alpha_2)$	0	1	1	0	0	0	1	1	-Vdc
$(\pi + \alpha_2)$ to $(2\pi - \alpha_2)$	0	1	1	0	0	1	1	0	-2Vdc
$(2\pi - \alpha_2)$ to $(2\pi - \alpha_1)$	0	1	1	0	1	1	0	0	-Vdc
$(2\pi - \alpha_1)$ to 2π	1	1	0	0	1	1	0	0	0