Modeling and Simulation of Nonvolatile Memory Based on copper sulfide

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Abstract

The memory cells has become one of the computer basics electronic components, especially nonvolatile ion-dependent growth of filament or so called Conductive Bridge Random Access Memory (CBRAM) type. The memory cells in this work is focused on using copper sulfide as ionic compound Cu_2S, the model proposed to identify the behavior of the cell in terms of voltage and current. The model cell is then simulated in order to extract the variables that affect the behavior of the cell and the factors which can be identify the optimal dimensions and specifications in terms of their small size and minimum power dissipation as possible at the same time. The simulation results show that the best thickness of the cell is about 20 nm with a radius equal to 10 nm, These dimensions of the cell has a resistance ratio of high resistance state HRS to low resistance state LRS(Roff / Ron) which correspond to different logic is about 10^{14}.

Keywords: Ionic Memory, Switching Memory, CBRAM.

نمذجة ومحاكاة ذاكرة خزن لافولتائية باستخدام مركب كبريتيد النحاس Cu_2S

الخلاصة

ان خلايا الخزن أصبحت من المكونات الأساسية لأجهزة الحاسوب، وخصوصا اللافولتائية منها وأحد انواعها الواعدة مستقبلا هي خلايا الخزن ذات الخاصية الايونية والمعتمدة على نمو الفتيلة. في هذا البحث تم التركيز على استخدام هذا النوع من الخلايا اللافولتائية ذات الوصول العشوائي من النوع الايوني باستخدام مركب كبريتيد النحاس وتم اقتراح نموذج بحيث يمكن من خلاله التعرف على تصرف الخلية من حيث الفولتية والتيار. ومن هذا النموذج ايضا يمكن محاكاة هذه الخلية لكي تستنتج المتغيرات التي تؤثر على تصرف الخلية واستخراج العوامل العديدة والتي من خلالها يمكن التعرف على مواصفاتها المثلى مثل صغر الحجم واقل قدرة مستهلكة بنفس الوقت. أظهرت نتائج المحاكاة إن أفضل سمك للخلية هو بحدود 20 نانوميتر وبنصف قطر مقداره 10 نانوميتر، وقد تبين إن هذه الإبعاد تكون نسبة مقاومتها وهي في حالة الإطفاء إلى حالة الإغلاق هي بحدود 10^{14}.

الكلمات الدالة: الذاكرة الأيونية، ذاكرة التحويل، الخلايا اللافولتائية ذات الوصول العشوائي.

Introduction

One of the promising technologies under development or next generation of non-volatile memory is the Conductive Bridging Random Access Memory (CBRAM) which utilizes the reversible switching of an electro resistive dielectric between two conductive states which means of storing logical data one and zero [1]. Non-volatile memories based on phase transformation, reversible defect generation/recombination, filament and metallic Nano-wire growth/etch are being extensively studied as an alternative to floating gate based flash memory devices

currently in use in stick memories and other applications[2].The switching is attributed to the electrochemical growth and dissolution of Cu or Ag Nano-sized filament[3,4]. The ultimate nonvolatile data memory (NVM) should display characteristics such as high-density, low cost, fast write, low energy operation, and high performance with respect to endurance and retention[3].

Conducting bridge random-access memory (CBRAM), also named programmable metallization cell solid-electrolyte memory technology which is promising for future nonvolatile memory device application[5].

In Figure (1) the CBRAM switching mechanism is depicted, which is based on the polarity dependent electrochemical deposition and removal of metal filament in a thin solid state electrolyte film. The ON-state is achieved by applying a positive bias larger than the threshold voltage Vth at the oxidizable anode resulting in redox reactions driving Agions in the chalcogenide glass. This leads to the formation of metal rich clusters, which form a conductive bridge between both electrodes. The device can be switched back to the OFF state by applying an opposite voltage. In this case, the metal ions are removed, which in turn erases the conductive bridge[6].

Two-terminal resistive switches, are electronic circuits which can extend the functional scaling of integrated circuits beyond CMOS, and offer non-volatility and 3D integration potential[7].
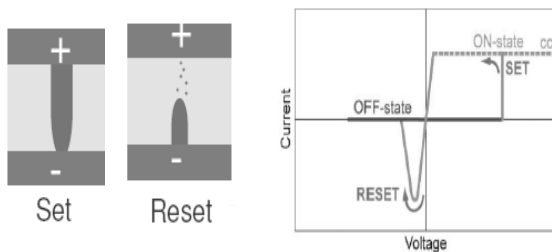
counter electrode or anode (Cu,Ag) included. Where the bottom represent the inert electrode or cathode (pt,w), the memory cell estimated as a general structure as shown in Figure (2), when positive voltage applied to the anode (top electrode) the filament start growing from the cathode through the solid electrode solid layer SL until the filament length reach the anode and the switching state happen to low resistance state (LRS), this mechanical sequence can be translated into equivalent circuit as shown in Figure (3). The model proposed uses the filament resistance R_{fil} connected in series with the ionic resistance R_{ion}, the bottom current source represent the interface between SL layer and filament, where the other current source correspond to SL layer and anode interface. This connection is also connected in parallel with the third current source which corresponds to tunnel current when the gap is small enough to switch the cell into ON state or LRS. The interfaces current source represents the electron transfer reaction at the boundaries. This method of representation gives acceptable results describing the behavior of the cell, assuming that constant filament radius with cylindrical shape approximation. Really the filament shape has Cone shape but for simplicity we can use cylindrical shape with acceptable results [5]. Also the electrodes resistance is included as R_{el} .
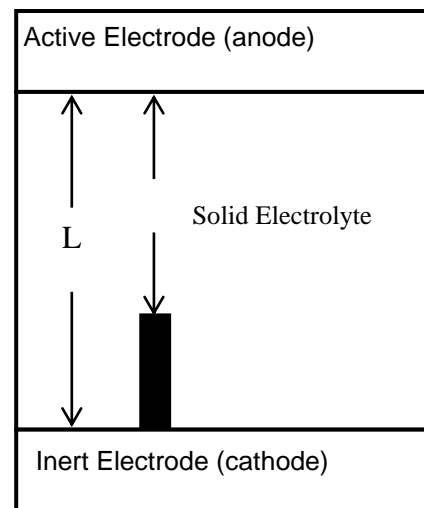

Fig. 1. Bipolar filamentary CBRAM structure

Modeling

In this work model has been used to predict the behavior of memory cell with bipolar properties. The property tunneling gap and electrochemical growing filament with the

Fig. 2. Memory cell proposed model

Figure (3) represents the equivalent circuit of the proposed model cell, when the positive voltage with respect to inert electrode is applied to the cell, the filament is growing to the top, then the resistance R_{ion} decreases according to resistivity law [3],

$$R_{ion} = \rho_{se}\, \frac{x}{A} \dots\dots\dots\dots\dots\dots\dots\dots\dots\dots (1)$$

Where ρ_{se} is the solid electrolyte resistivity, at the same time the filament resistance R_{fil} will be increased and can be given by:

$$R_{fil} = \rho_{fil}\, \frac{L-x}{A} \dots\dots\dots\dots\dots\dots\dots\dots\dots (2)$$

Where ρ_{fil} is the filament resistivity, when the low resistance state LRS is reached, the value of gap x will be at minimum distance which will cause the tunneling current between the two electrodes, the cell will be switched to the ON state.
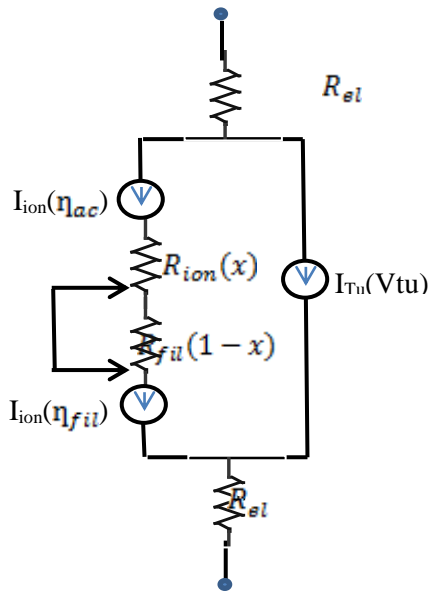

Fig. 3. Memory cell equivalent circuit

When a positive voltage applied to the anode, the filament will grow gradually from the cathode electrode according to Faraday's Law, the X growth/dissolution rate is [8],

$$\frac{\partial x}{\partial t} = -\frac{M_{me}}{z\, e\, \rho_{m,Me}} J_{Me^{z+}} \dots\dots\dots\dots\dots\dots\dots (3)$$

Where, $J_{Me^{z+}}$ is the ionic current density, z is the charge transfer number, M_{me} is the atomic

mass, $\rho_{m,Me}$ is the mass density of the deposited material and e is the electron charge.

To calculate the amount of current source, the ionic current density $J_{Me^{z+}}$ represent the reaction between electrodes and solid electrolyte SL at the interface and can be described by Butler-Volmer equation[3],

$$J_{Me^{z+}} = J_{BV}\,(\eta) = 2\, j_\circ\, sinh\left(\frac{ze}{2KT}\,\eta\right) \dots\dots\dots (4)$$

$j_\circ$ is the transfer current density [9], and η is the over potential ,the last equation describes the oxidation – reduction reaction at interfaces. Also the Mott-Gurney law[10], which is describing the ion hopping transport shows the same mathematical dependence and thus could also explain the nonlinear switching dynamics .

Due to charge neutrality the ionic current density at the active electrode $J_{BV}\,(\eta_{ac})$ and $J_{BV}\,(\eta_{fil})$ are equal to each other.

$$J_{BV}\,(\eta_{ac}) = J_{BV}\,(\eta_{fil}) \dots\dots\dots\dots\dots (5)$$

Where

$$J_{BV} = \frac{I_{ion}}{A} \dots\dots\dots\dots\dots\dots\dots\dots\dots\dots (6)$$

$$I_{ion} = -2\, jo\ \ A_{fil}\, sinh\left(\frac{ze}{2KT}\eta_{fil}\right) = 2\, jo\ A_{ac}\, sinh\left(\frac{ze}{2KT}\,\eta_{ac}\right) \dots\dots\dots\dots\dots\dots\dots (7)$$

Solving Equation (5) for η_{ac}:

$$\eta_{ac} = \frac{2KT}{ze}\, sinh^{-1}\left(-\frac{A_{fil}}{A_{ac}}\, sinh\left(\frac{ze}{2KT}\eta_{fil}\right)\right) \dots (8)$$

Where A_{fil} and A_{ac} is the filament and active electrode area respectively. Using Kirchhoff's first law and the equivalent circuit shown in Figure (3), then the total cell current can be calculated as:

$$I_{cell} = I_{TU}(V_{TU}) + I_{ion} \dots\dots\dots\dots\dots (9)$$

Substituting for I_{ion} equation

$$I_{cell} = I_{TU}(V_{TU}) + I_{BV}\,(\eta_{fil}) \dots\dots\dots\dots (10)$$

Where V_{TU} is the tunnel voltage, and can be calculated as the voltage drop across the solid electrolyte SL only as follow,

$$V_{TU} = \eta_{ac} - \eta_{fil} + I_{BV}\left(\eta_{fil}\right) R_{ion}(x) \dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots (11)$$

The tunneling current can be calculated from Simmons formula [11], and in order to simplify the mathematical solution

$$R_{fil} = R_{ion}$$, so

$$I_{TU} = \frac{e\,A_{fil}}{2\pi h x^2}\left\{\left(\varphi_o - \frac{eV_{TU}}{2}\right)e^{-\frac{4\pi x}{h}\sqrt{2m_{eff}}\sqrt{\varphi_o - \frac{eV_{TU}}{2}}} - \left(\varphi_o + \frac{eV_{TU}}{2}\right)e^{-\frac{4\pi x}{h}\sqrt{2m_{eff}}\sqrt{\varphi_o + \frac{eV_{TU}}{2}}}\right\}$$

………………………………………….......(12)

Where φ_o is the barrier height and $m_{eff} = m_r.m_o$ is the electron effective mass of SL. Finally the overall memory cell voltage can be founded by combining the above equations.

$$V_{cell} = V_{TU} + I_{cell}[R_{fil}(x) + R_{el}] = f(x, \eta_{fil})$$
……………..…………………………….(13)

Equation (13) is a general solution for memory cell describing the relation between voltage and current as a function of gap x.

Simulation

Starting with the initial V_{cell} and with gap X equal to the cell thickness L, Equation (13) can be numerically solved, just η_{fil} calculated and substituted into Equation (5), $J_{ion} = J_{BV}(\eta)$ can be found, by solving the differential Equation (3), the new value of X

can be founded and by repeating these steps in new time step the voltage and current of the memory cell can be founded along with the ionic and tunneling current , also the resistance of the cell can be calculated from these simulation steps.

The voltage cell (V_{cell}) is varied with the time according to the set or reset state, for the setting voltage when the compliance current is reached the threshold voltage of the cell enter into ON state or LRS. Opposite the reset voltage, the cell will go to the OFF state or HRS. By these sets of equations the behavior of the memory cell can be modeled and simulated.

Results

In this work as a study case based on using Copper Sulfide Cu2S as a solid layer SL, Cu2S is known to be a p-type defect semiconductor with shallow Cu vacancy acceptors, and have a band gap of 1.2 eV and an electron affinity of 4.3 eV[9].

For simplicities the active electrode and filament area is equal to each other Aac = Afil = π rfil2 where the latter is the filament radius. The CU2S parameters used in this simulation is taken from reference 8,12,13 and 14 as shown in Table (1).

Table 1. The CU2S parameters

	Z	ρ_{m,c_u}	M_{c_u}	T	φ_o	m_r	$\rho_{o,el}$	j_o
	2	8.95 g/cm³	1.06 * 10⁻²²	300k	0.8 e.v	0.86	0.004 Ω/m	10⁻²
Ref.	8	8	8	------	14	14	13	8

A triangular wave is applied to cell with amplitude equal to one volt and with a duration time equal to 4 second as shown in Figure (4), this input voltage used to study the memory cell response voltage versus current. The current compliance is chosen to 10 µA to prevent the cell breakdown.

Figure (5) shows the simulation results for different filament radius 2,5,10, and 20 nm with cell thickness equal to 20nm as shown in legend, it is clear that when the filament radius is increased or the active electrode area increased the ratio of switching R_{OFF}/R_{ON} decreased, for R =2 nm the ratio is about 60 x

10^3 and increasing the value of R will tend to decrease the ratio of R_{OFF}/R_{ON} and for R=20 the ratio is near zero value, it should be noted that the filament radius r = 5nm will give a ratio of about 10^3 which seems to be a good value in order to compare between the ON and OFF state i.e '1' and '0' logic.

The role of ion current can be seen in the building of conductive bridge or filament as shown in Figures (6) and (7), the ionic current is very small between 0 and 0.8 second and enough to construct the filament at switching voltage V_t equal to 0.4 volt, where the tunneling current plays a basic role for

switching the memory cell from OFF to ON as shown in Figure (8).

The gap x which represent the filament growth is not depend on the filament radius or the thickness of the memory cell and only depend on the ionic current with the time constructing the filament. Figure (9) shows the relation of Set and Reset states with time in second for a different radiuses, for setting the cell to ON state x is decreased from the cell thickness L to minimum value, the minimum time needed for switching the cell to ON state is about 0.4s.
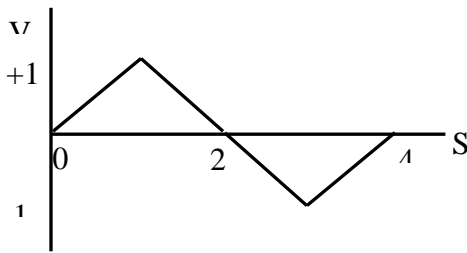
Fig. 4. Cell input voltage
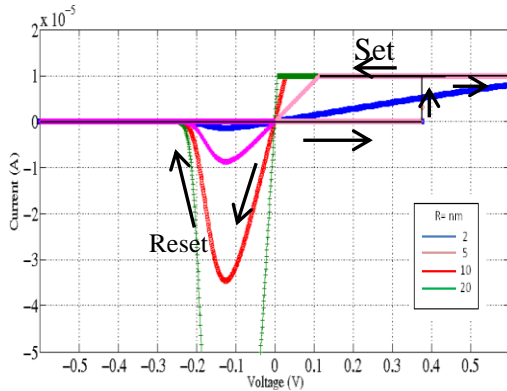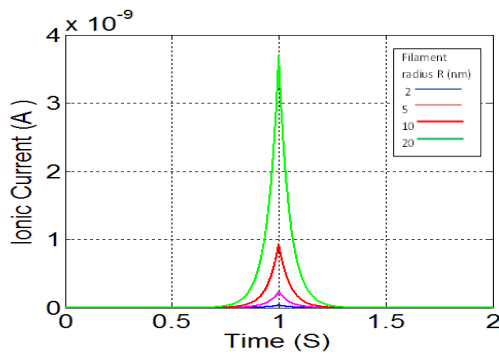

Fig. 5. Current Voltage Characteristics of Cu$_2$S

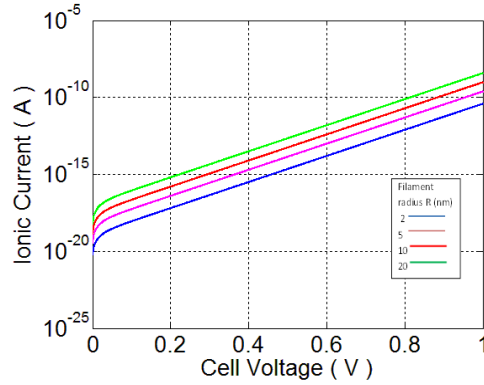**Fig.6.** Different ionic current with filament radius

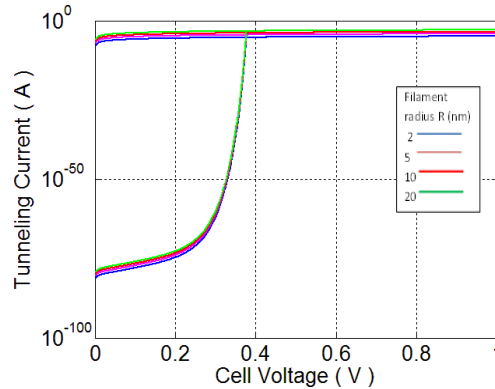

Fig. 7. Ionic current of Cu$_2$S Cell

Fig. 8. Tunneling Current of Cu$_2$S Cell

Cell Thickness

From Equation (1) the cell resistance is depending on the filament radius only as shown in Figure (10), it is noticed that increasing cell thickness will decrease the value of cell reset current as shown in Figure(11). The cell of 20nm thickness will need about 140µA for resetting the cell from LRS to HRS, while the cell of 30nm thickness will need about 25µA for resetting the cell. Also from Figure (11), it is clear that by increasing the cell thickness the set voltage will be increased.
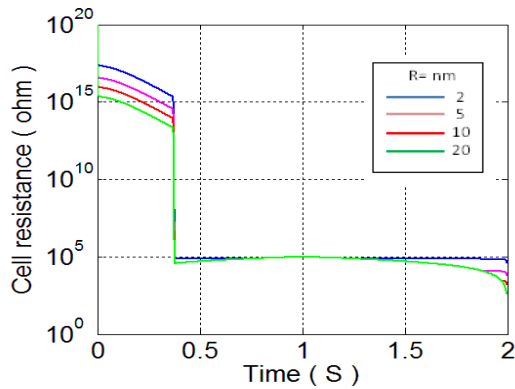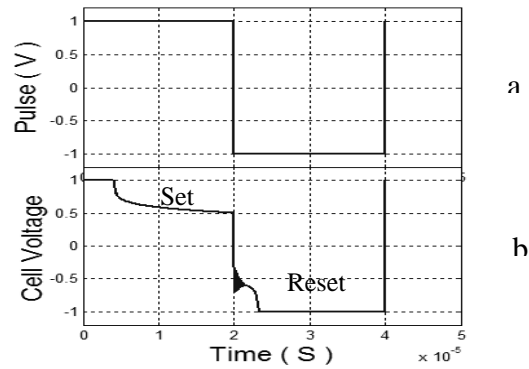
Fig.10. Cell resistance with different radius

Fig.12. a. Square pulse, b. Cell voltage

Conclusion

The results of non-volatile Cu_2S memory cell shows that increasing the cell width (effective area or filament radius) will have great effect on the ratio of Roff / Ron and does not affect the switching voltage (threshold voltage). The best acceptable value in terms of the distinction between logic zero and one is the filament radius of 10nm and the ratio of high to low resistance 10^{14}. The factor that affects the value of cell threshold voltage is the cell thickness and has a small effect on the ratio Roff / Ron. The optimal thickness of the cell is located between (20 – 30)mm. The memory cell size must be chosen according to the optimized cell thickness and width and according to acceptable switching voltage and the ratio of HRS to LRS.
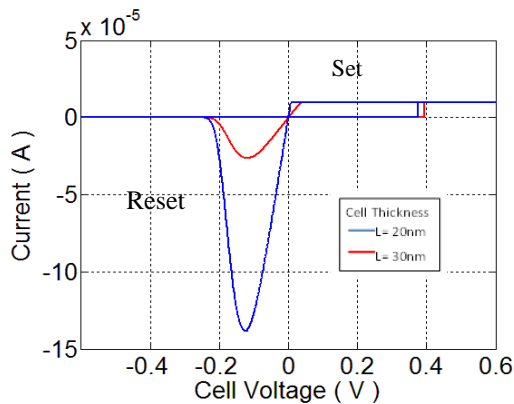

Fig.11. Characteristic with different cell thickness

Switching Time

Measured from applying a square pulse to the cell in series with current limiting resistance. When the pulse is in high state and the filament length is zero (X=L) there is no current flow through the cell so all applied pulse is on the cell then the cell voltage is the same as input pulse, just the filament is constructed the resistance is decreased to the low state (ON) and half of the input voltage drop across the limiting resistance then the voltage decreased to minimum as shown in Figure (12). The switching time can be measured between starting time and when the cell voltage dropped, the measured time from the figure is about 5μs and this time is fast and very small compared with other type of memory which is more than 100μs.

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