

## ELIMINATING HARMONICS IN A FIVE LEVEL INVERTER BY OPTIMIZED BOTH SWITCHING ANGLES AND DC LINK VOLTAGE

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### ABSTRACT

This paper presents design and analysis of a single phase multilevel inverter by optimizing both switching angles and DC link voltage of a cascaded inverter. The switching angles and dc link voltage are chosen such that to minimize the total harmonic distortion of the output voltage. The main power devices are switched only once per cycle, so that to overcome the switching loss problem, as well as electromagnetic interference (EMI) problem, a method is given to determine the optimum value of the switching angles and the value of the dc link voltage. Theoretical analysis and simulation of a single phase 5-level cascaded inverter are introduced with a wide range of modulation index

**KEYWORDS:** multilevel inverter, optimized switching angles, cascaded inverter, DC link voltage

$d_1, d_2, \dots, d_s$	Voltage increment portions of $V_{dc1}$
$E_1, E_2, \dots, E_s$	Voltage level of each H-bridge
$H(n)$	Harmonic amplitude
$M_f$	Frequency ratio
$M$	Modulation index
$m$	Number of levels
$n$	Harmonic order

$S_1, S_2, \dots, S_n$	Main switching device
$s$	Number of DC source
$V_L^*$	Amplitude command of the inverter output voltage $H_n$
$V_{Lmax}$	Maximum attainable amplitude of the converter
$V_{AN}$	Single phase output voltage
$\alpha_1, \alpha_2, \dots, \alpha_n$	Switching angles

## INTRODUCTION

Multilevel topologies<sup>[1-4]</sup> and modulation techniques have been developed and applied in high power system. With the requirement of quality and efficiency in high power systems with the limitation of high power device switching speed, low total harmonic distortion (THD) and low switching frequency are desirable. By applying appropriate modulation scheme these two aim can be achieved. The harmonic elimination technique in <sup>[5-8]</sup> initiates the concept of achieving harmonic reduction with selected harmonic elimination there are three possible optimized techniques to reduce harmonics order <sup>[3]</sup> :1) assuming equally spaced steps, steps heights are optimized 2) assuming steps of equal heights, their spacing are optimized 3) optimized both heights and spacing, in this work third method is used.

### Multilevel inverters

The multilevel inverter<sup>[9-10]</sup> unique structure allows them to reach high voltages with low harmonics. The general function of multilevel inverter is to synthesize a desired voltage from several levels of dc voltages , for this reason multilevel inverter can easily provide high

power applications. As the number of levels increases, the synthesized output waveform has more steps , which produce a staircase wave that approaches a desired waveform, also the harmonic distortion of the output waveform decreases, approaching to zero as the number of level increase . There are three types of multilevel inverter 1) Diode-Clamped Multilevel inverter. 2) Flying-capacitor Multilevel Inverter. 3) cascaded inverter .The popular type structure of the multilevel inverters is the cascaded H-Bridge type.

### Cascaded H-Bridge inverter with separate DC source

This type of inverter consists of full bridge or H-Bridge inverters connected in series and the output voltage is equal to the sum of the outputs of all H-bridge inverters. Each inverter may have independent source obtained from either battery, solar cell, or fuel cell, and the configuration recently becomes popular in ac power supplies, and adjustable speed drive applications. This type has less components than the other inverter types. Fig. (1) shows a Structure of single phase m-level cascaded inverter, in which each DC source is associated with single phase

H-bridge inverter, the output of each H-bridge can be controlled by four switches and the DC source. The output phase voltage levels are defined by  $m=2s+1$ , where  $m$  is the number of levels and  $s$  is the number of DC sources.

**Optimized harmonics stepped waveform**

By using Fourier series expansion of the (stepped) output voltage waveform of the multilevel inverter shown in fig.(2), the output voltage  $V_{AN}(\omega t)$ , Fourier coefficients can be written as [3,6,8]:

Since the waveform in Fig.(2) has odd symmetry, therefore the Coefficients  $a_n$  and  $a_0$  are equal zero for all values of  $n$ .

$$b_n = \frac{1}{\pi} \int_0^{2\pi} f(\omega t) \sin(n \omega t) d\omega t$$

Where  $f(\omega t) = V_{AN}(\omega t)$

$$b_n = \begin{cases} \frac{4}{\pi} \int_0^{\frac{\pi}{2}} f(\omega t) \sin(n \omega t) d\omega t \\ 0, \text{ for even } n, n=2,4,6 \dots \end{cases}$$

$$V_{AN}(\omega t) = \sum_{1,3,5}^{\infty} b_n \sin(n \omega t) \text{ ----- (3)}$$

From equation (2), and Fig. (2)

$$b_n = \frac{4}{\pi} \left[ \int_{\alpha_1}^{\alpha_2} E_1 \sin(n \alpha) d\alpha + \int_{\alpha_2}^{\alpha_3} E_2 \sin(n \alpha) d\alpha + \dots + \int_{\alpha_s}^{\pi/2} E_s \sin(n \alpha) d\alpha \right] = \frac{4}{n\pi} \left[ E_1 \cos(n\alpha_1) + (E_2 - E_1) \cos(n\alpha_2) + \dots + (E_s - E_{(s-1)}) \cos(n\alpha_s) \right] \text{ -----(4)}$$

From Figures (1) and (2), the following relationships can be found

$$\begin{aligned} V_{dc1} &= E_1 \\ V_{dc2} &= E_2 - E_1 \\ V_{dcS} &= E_S - E_{(S-1)} \dots \dots \dots (5) \end{aligned}$$

For variant dc link  $V_{dc2} = V_{dc1} + d_1$ ,  $V_{dc3} = V_{dc1} + d_2, \dots, V_{dcS} = V_{dc1} + d_S$  ----(6)

voltage source the following assumptions can be introduced :

As  $V_{dc1}$  reference, then substitute equation(6) in equation (4) results :-

$$b_n = \frac{4}{n\pi} \left[ V_{dc1} \cos(n\alpha_1) + (V_{dc1} + d_1) \cos(n\alpha_2) + \dots + (V_{dc1} + d_S) \cos(n\alpha_s) \right] \text{ .....(7)}$$

It is convenient to introduce the per unit value for  $V_{dc1}$ , then equation(7) becomes:

$$b_n = \frac{4}{n\pi} \left[ \cos(n\alpha_1) + (1+d_1)\cos(n\alpha_2) + \dots + (1+d_s)\cos(n\alpha_s) \right]$$

Therefore , the output voltage can be written as :

$$V_{AN}(\alpha) = \left( \frac{4}{n\pi} \left[ \cos(n\alpha_1) + (1+d_1)\cos(n\alpha_2) + \dots + (1+d_s)\cos(n\alpha_s) \right] \right) \sin n\alpha \tag{8}$$

According to fig.(2)  $\alpha_1$  to  $\alpha_s$  must satisfy the following condition  $\alpha_1 < \alpha_2 < \dots < \alpha_s < \pi/2$ . The two predominant methods in choosing the switching angles  $\alpha_1, \alpha_2, \dots, \alpha_s$  include: 1) eliminating the lower frequency dominate harmonics and 2) minimizing the THD. The more popular of the two techniques is to reduce THD and to eliminate the lower dominate harmonics and then filter the higher residual frequency. From equation (8), the amplitude of odd harmonic components for quarter-wave symmetry is:

$$H(n) = \frac{4}{n\pi} \left[ \cos(n\alpha_1) + (1+d_1)\cos(n\alpha_2) + \dots + (1+d_s)\cos(n\alpha_s) \right] \tag{9}$$

The set of non-linear equations corresponding to (9) can be given as follows:

$$\left. \begin{aligned} & \frac{4}{\pi} [\cos(\alpha_1) + (1+d_1)\cos(\alpha_2) + \dots + (1+d_s)\cos(\alpha_s)] = H_1 \\ & \frac{4}{3\pi} [\cos(3\alpha_1) + (1+d_1)\cos(3\alpha_2) + \dots + (1+d_s)\cos(3\alpha_s)] = H_3 \\ & \frac{4}{5\pi} [\cos(5\alpha_1) + (1+d_1)\cos(5\alpha_2) + \dots + (1+d_s)\cos(5\alpha_s)] = H_5 \\ & \dots \\ & \frac{4}{n\pi} [\cos(n\alpha_1) + (1+d_1)\cos(n\alpha_2) + \dots + (1+d_s)\cos(n\alpha_s)] = H_n \end{aligned} \right\} \tag{10}$$

The set of nonlinear equation (10) can be solved by iterative methods such as Newton-Raphson method[ 3]or by using trigonometric identities to expand the terms  $\cos(n\alpha_n)$  and then using resultant theory<sup>[7]</sup> .

The switching angles may also be solved to minimize the THD. The THD for the voltage waveform may be defined as <sup>[4]</sup>.

$$THD (\%) = \frac{\sqrt{\sum_{n=2}^{\infty} (H_n)^2}}{H_1} \tag{11}$$

In general the modulation index M of the sinusoidal pulse width modulation (SPWM) which is the ratio of the modulating signal amplitude to the carrier signal amplitude, while for the

specified multilevel inverter case the modulation index is defined as follow [3]:

$$M = \frac{V_L^*}{V_{Lmax}} \quad \text{-----(12)}$$

### FIVE LEVEL INVERTER

A simple example to verify the set of equations (10) is a five level inverter ( $m=5=2S+1$ ) is constructed with two dc source ( $S=2$ ), since each separate dc source has two level +ve Vdc and -ve Vdc (two level) plus zero level, therefore two H-bridges with two switching angle equations can be written to eliminate the harmonic component .

$$\cos(\alpha_1) + (1+d_1)\cos(\alpha_2) = \frac{SM\pi}{4} \quad \text{---- (13)}$$

$$\cos(3\alpha_1) + (1+d_1)\cos(3\alpha_2) = 0 \quad \text{--(14)}$$

$$\cos(5\alpha_1) + (1+d_1)\cos(5\alpha_2) = 0 \quad \text{---(15)}$$

Solving equations (13-15), table (1) shows a various switching angles according to modulation index and the corresponding voltage THD.

### SIMULATION OF SINGLE PHASE MULTILEVEL CASCADED INVERTER

Due to the advances in Simulation packages ,theoretical simulation becomes very important before any step of implementations of any electrical device .

One of the effective packages in electrical circuits and devices is the OrCAD [11], this packages can deal with many types of devices that located in their library. Appendix 1 shows the circuit diagram of 5-level using OrCAD. From table 1, when the switching angles  $\alpha_1=16.23^\circ$  ,  $\alpha_2=51.56^\circ$  ,  $d_1=-0.27$  , the THD has minimum value. These values of angles are chosen for design of the inverter. The gate pulses of the MOSFET's are shown in fig(3), fig(4) shows the simulation output voltage of 5-level inverter. Fig(5) shows the spectrum analysis of the output voltage of the inverter, and table (2) shows the magnitude of the harmonics components up to 21<sup>th</sup>.

### CONCLUSIONS

For all values of n , from equation (1), the time function in terms of Fourier series is given as :

In this paper optimum values of switching angles and DC source voltages were obtained in order to eliminate the lowest order harmonic (LOH) and to minimize THD of the output voltage waveform of a single phase 5-level cascaded inverter. The switches are closed and open one time per cycle. The simulation of this inverter was proved that the inverter has low THD (18%) with respect to traditional PWM inverter without using any filter. The analysis of this waveform shows that the LOH of this type of strategies can be found by the formula  $3S+1$  for odd number of DC sources and  $3S+2$  for even number of DC sources. For 5-level the LOH equals  $3*2+1=7^{\text{th}}$  and for 7-level the LOH equals  $3*3+2=11^{\text{th}}$  harmonic. This type of modulation technique is suitable for the applied low pass filter in order to eliminate unwanted components of output waveform. Multilevel modulation strategy is considered more efficient than PWM one, due to very low power loss raised by the switching of the power electronics devices. Besides that, the LOH amplitude in multilevel inverter is much lower than the  $M_f$  order harmonic in PWM technique, this leads to say that any order filter can remove the harmonics from the output

waveform of multilevel. While in PWM inverter requires more complicated filter to reduce the value of higher order harmonics to zero.

## REFERENCES

- 1- F.Z peng, j-S lai, "Multilevel Converter- A New Breed of power converter "IEEE Trans. on Ind. Appl., Vol.32, No.3, May/June 1996, pp.509-517.
- 2- A. Nabae, I. Takahashi, H. Agaki, "A New Neutral-Point-Clamped PWM Inverter," IEEE Transactions on Industry Applications. Vol.IA-17, No.5, Sep./Oct., 1981, pp.518-523.
- 3- P. M. Bhagwat and V. R. Stefanovic, "Generalized Structure of a Multilevel PWM Inverter," IEEE Transactions on Industry Applications, Vol.IA-19, No.6 Nov./Dec., 1983, pp.1057-1069.
- 4- Mohammed H. Rashid "power electronic: circuit device, and application " Prentice -Hill, USA, 2004
- 5- S. R. Bowes, "New Sinusoidal Pulse width-Modulated Inverter," Proc.IEE, Vol.122, No.11, Nov, 1975.
- 6- H.S.patel, R.G. Hoft, "Generalize techniques of harmonics Elimination

- and voltage control in thyristor inverter :part I –Harmonic Elimination “IEEE Trans. on Ind. Appl., Vol.IA.9,No.3, May /June , 1973,pp.310-371.
- 7- J.chiasson , L. Tolbert ,  
” Eliminating Harmonics in a multilevel converter using resultant theory “www.powerelec.ece.utk.edu/pubs/ pesc 2002
- 8- S.irisukprasert and Tian .H Liu “ optimum harmonic reduction with a wide range of modulation index for multilevel inverter ” www.cpes vt.edu /cpespubs/proceedings/ /2001.
- 9- L. M. Tolbert, F. Z. Peng, “Multilevel Converters for Large Electric Drives,” IEEE Transactions on Industry Applications, Vol.35, No.1, Jan/Feb, 1999, pp. 36-34.
- 10- Q.Jiang and T. A. Lipo “ Switching angel and DC link voltage for multilevel inverter “ Electric machines and power system , Vol.28, pp.605-612 ,2000.
- 11- OrCAD Release 9 Manual”, OrCAD, Inc,1999.

**Table (1) the output voltage THD corresponding to the switching angles and dc link voltage for 5-level inverter**

Modulation index M	$\alpha_1$ Degree	$\alpha_2$ Degree	$d_1$ P.U	THD %
1	13.43	48.95	-0.089	18.29%
0.95	14.43	50	-0.18	18.69%
0.9	16.23	51.56	-0.27	18.22%
0.85	17.58	53.41	-0.358	18.65%
0.8	19	55.86	-0.444	19.7%
0.75	20.53	59.48	-0.524	20.9%
0.7	22.12	65.50	-0.581	22.9%
0.65	23.92	82.04	-0.226	31.2%

**Table (2) magnitude of Fourier component**

Harmonic NO	Frequency (Hz)	Fourier component	Normalized component
1	5.000E+01	1.977E+01	1.000E+00
2	1.000E+02	3.426E-02	1.733E-03
3	1.500E+02	6.809E-02	3.444E-03
4	2.000E+02	2.634E-01	1.332E-02
5	2.500E+02	3.029E-01	1.532E-02
6	3.000E+02	3.439E-01	1.740E-02
7	3.500E+02	4.997E-01	2.527E-02
8	4.000E+02	3.791E-02	1.918E-03
9	4.500E+02	1.518E+00	7.677E-02
10	5.000E+02	4.436E-02	2.244E-03
11	5.500E+02	2.147E+00	1.086E-01
12	6.000E+02	6.407E-02	3.240E-03
13	6.500E+02	4.283E-01	2.166E-02
14	7.000E+02	1.612E-01	8.153E-03
15	7.500E+02	2.506E-01	1.268E-02
16	8.000E+02	3.868E-01	1.956E-02
17	8.500E+02	2.327E-01	1.177E-02
18	9.000E+02	1.448E-01	7.324E-03
19	9.500E+02	3.549E-01	1.795E-02
20	1.000E+03	6.658E-02	3.368E-03
21	1.050E+03	1.154E+00	5.836E-02

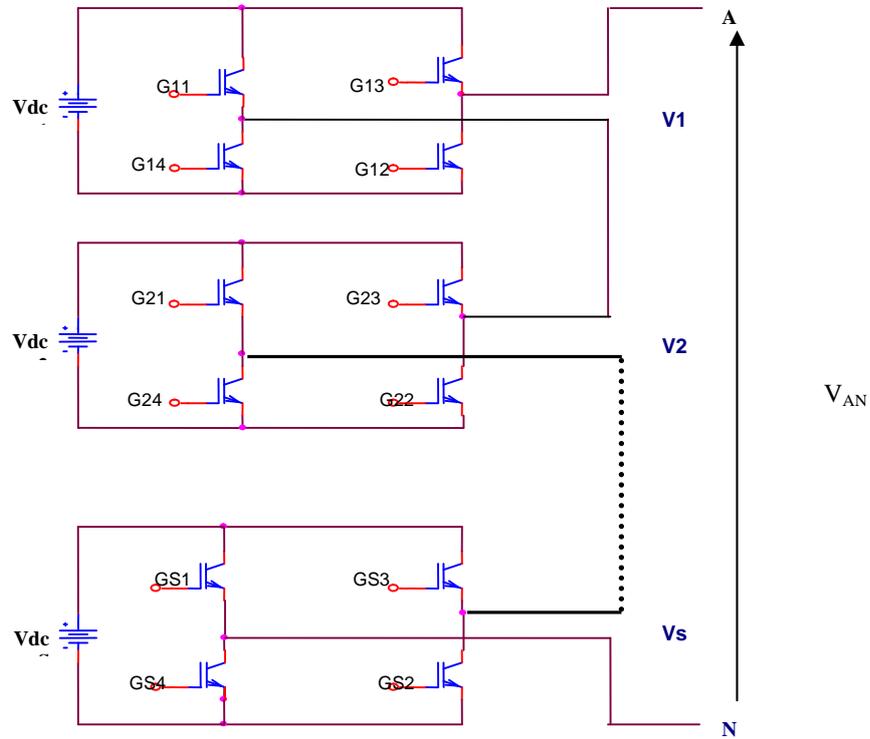
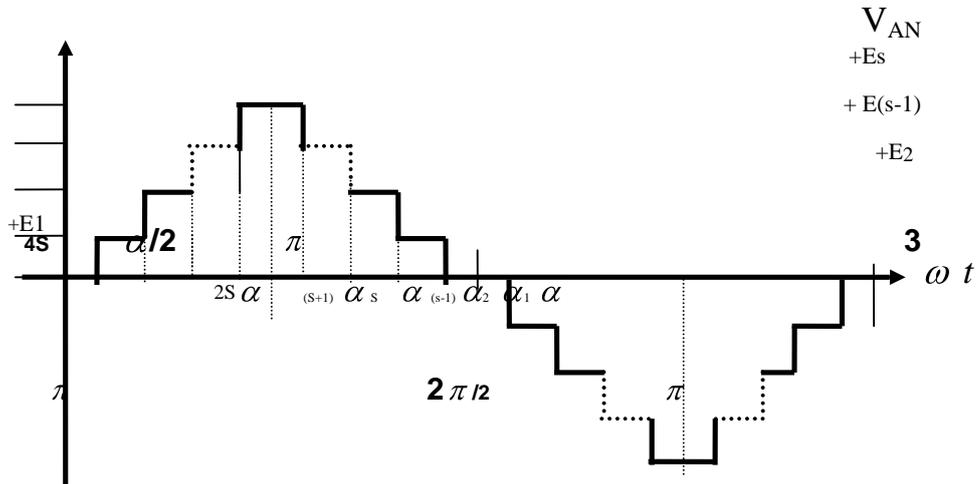
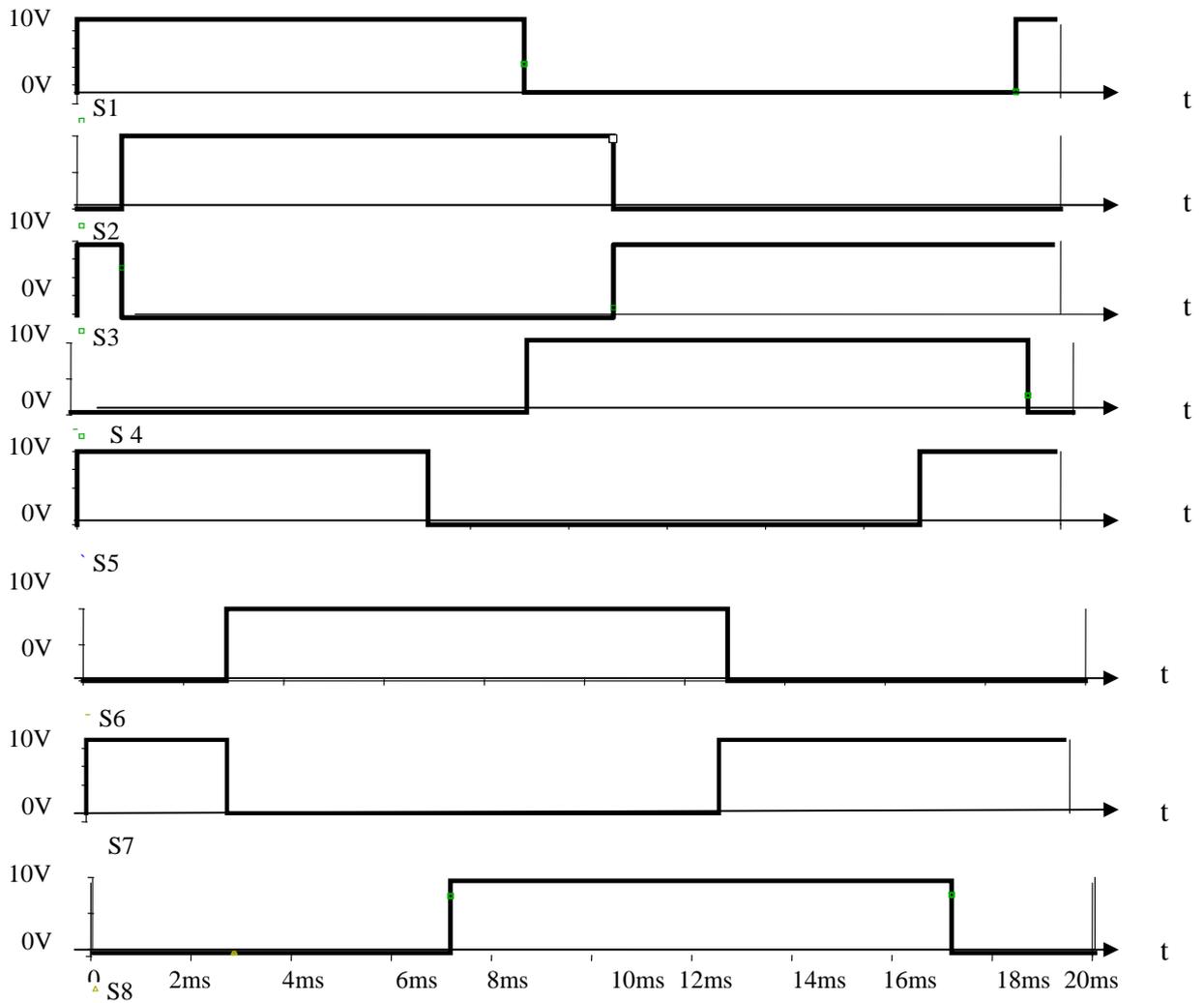


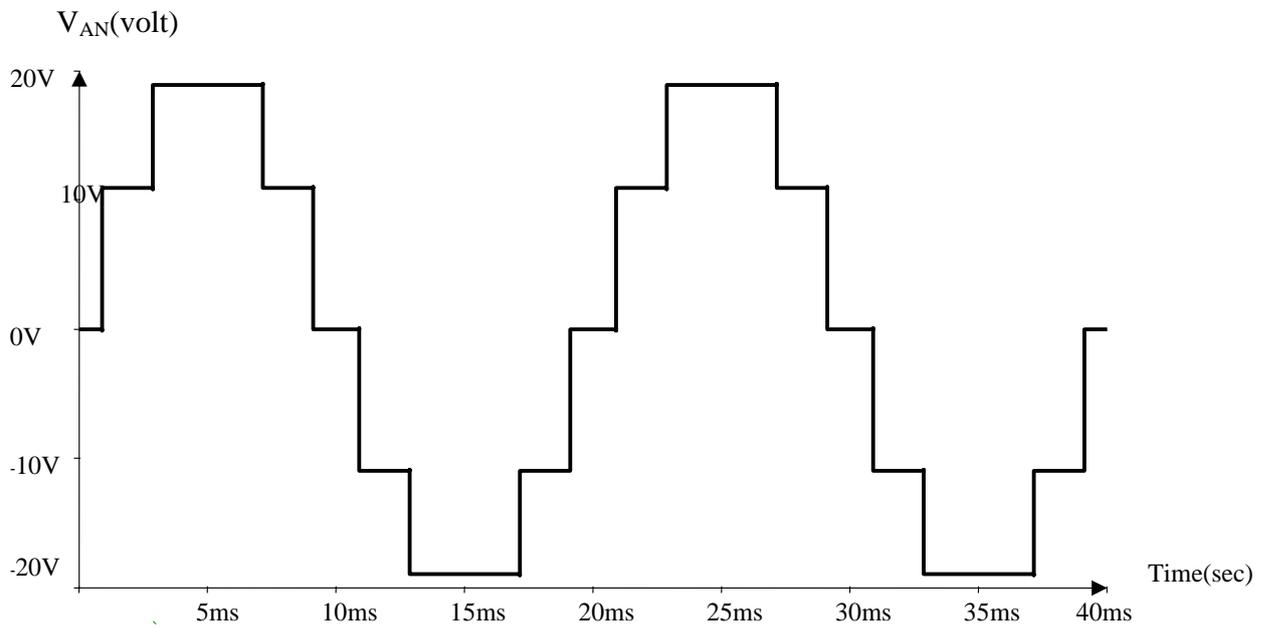
Fig (1) Structure of single phase m-level cascaded inverter



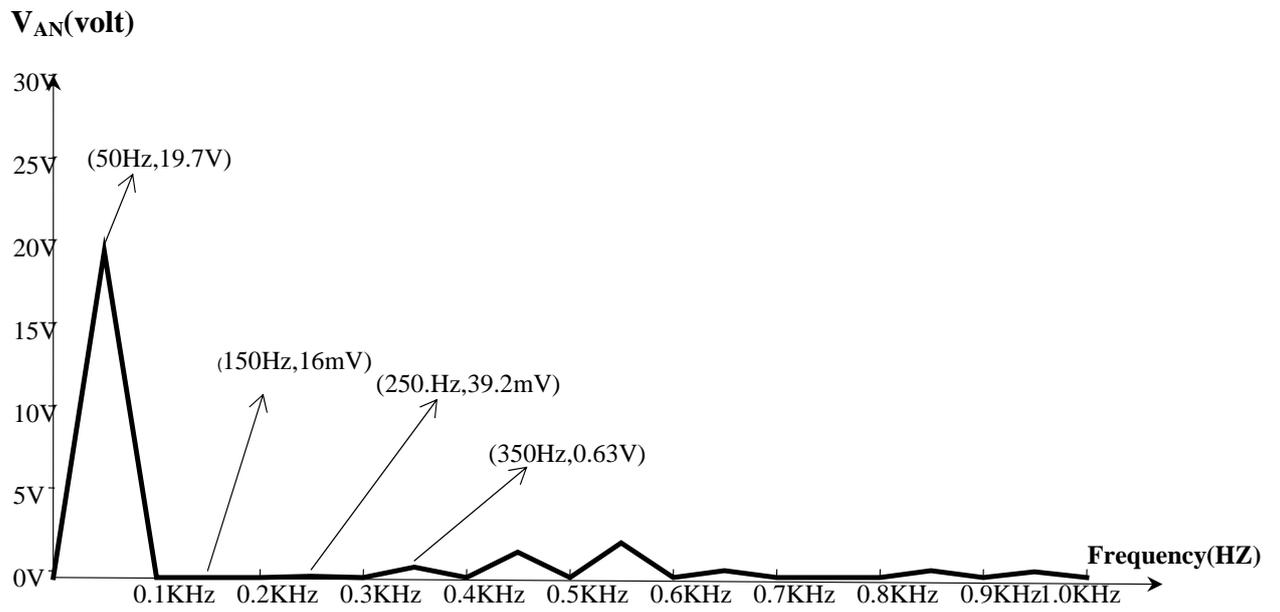
Fig(2) output voltage waveform of m-level inverter



**Fig(3) Gate switching voltage waveforms**

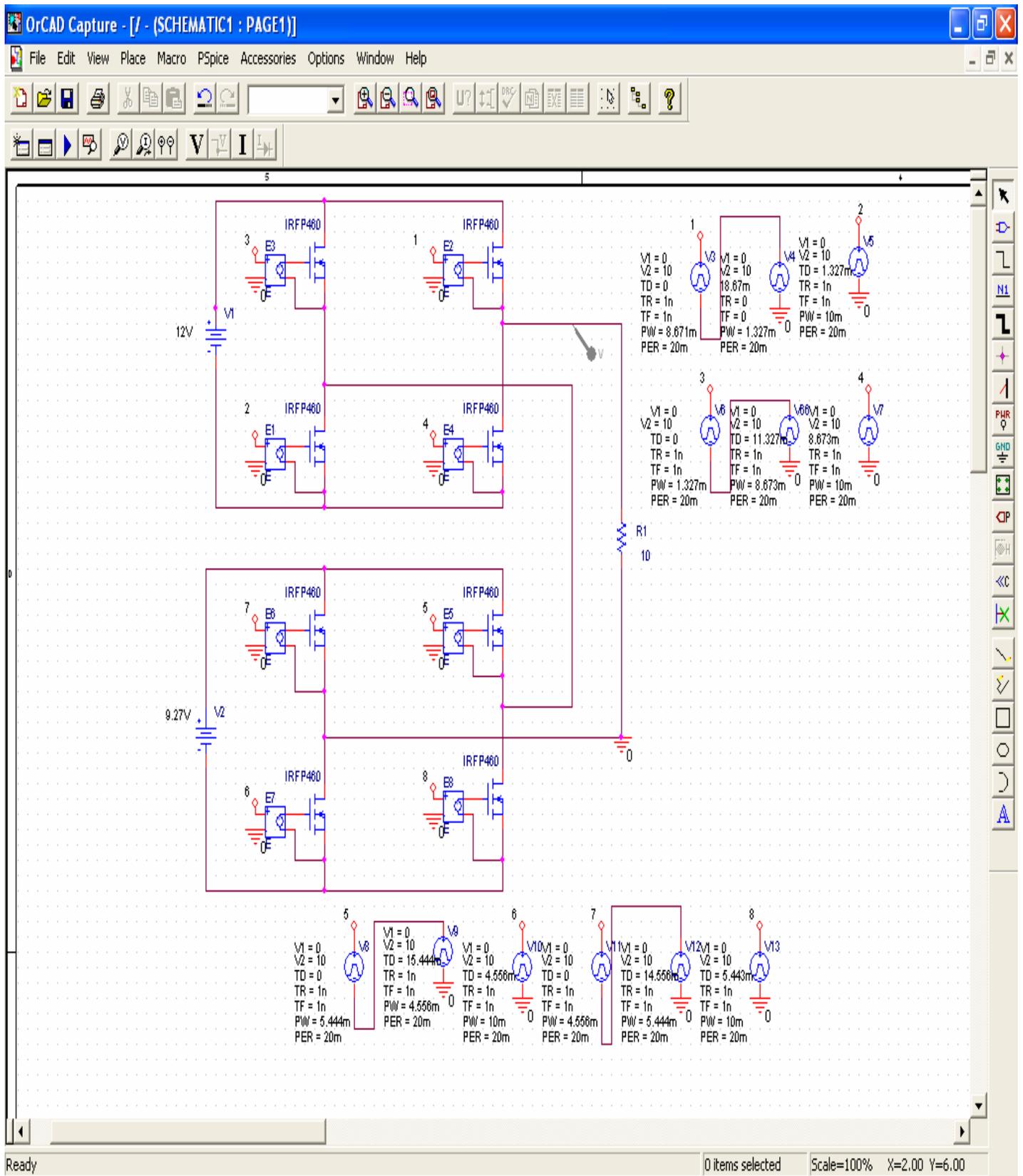


**Fig(4) Output voltage waveform of 5-level inverter with variant DC source**



**Fig(5) spectrum of the output voltage waveform**

### Appendix 1



إزالة التوافقيات للعاكس ذو المستوى الخامس باستخدام امثل زوايا تشغيل مصادر  
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الخلاصة

يتضمن هذا البحث تصميم وتحليل عاكس أحادي الطور متعدد المستويات باستخدام امثل قيم لزوايا تشغيل العناصر الالكترونية وفولتية وصلة التيار المستمر ليكون النشوة الكلي للتوافقيات في الفولتية الخارجة اقل ما يمكن، أن مفاتيح القدرة الرئيسية في الدائرة يتم تشغيلها مرة واحدة خلال كل دورة تردد تشغيل مما يقلل من المفاهيم الناتجة عن تشغيل المفاتيح والتخلص من مشكلة التداخل الكهرومغناطيسي، تم وضع طريقة لحساب القيم المثلى لزوايا التشغيل ومقدار فولتية وصلة التيار المستمر. تم تقديم تحليل نظري لعاكس ذي خمسة مستويات ولمدى واسع لعامل التضمين.

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